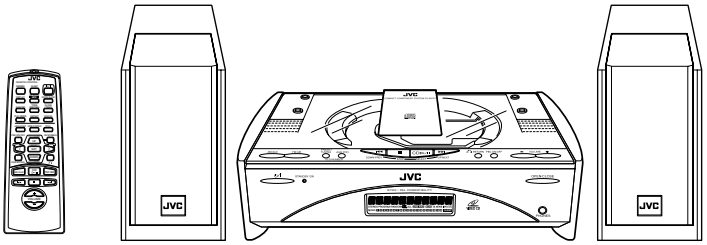
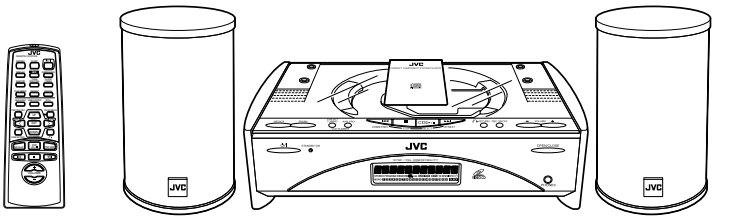
JVC

SERVICE MANUAL

COMPACT COMPONENT SYSTEM

FS-SD58V
FS-SD78V / FS-SD98V





Area Suffix

FS-SD58V

UB --------- Hong Kong
UF ---------- China
US ---------- Singapore

FS-SD78V / FS-SD98V

UF ---------- China
US ---------- Singapore

These models are different only speaker systems.
FS-SD78V and FS-SD98V are different only speaker cabinet.

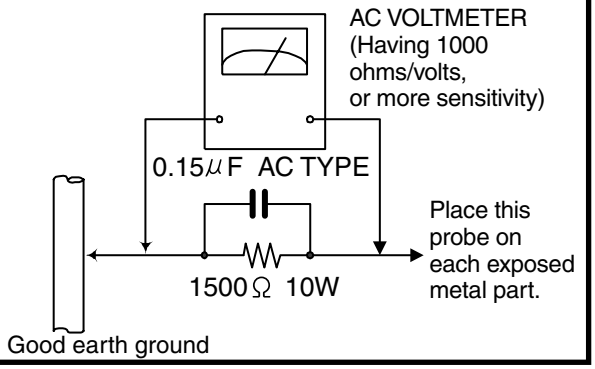
Contents

These models not have adjustment.

No.20882
Nov. 2000

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Important for Laser Products

1.CLASS 1 LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ **CAUTION** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.

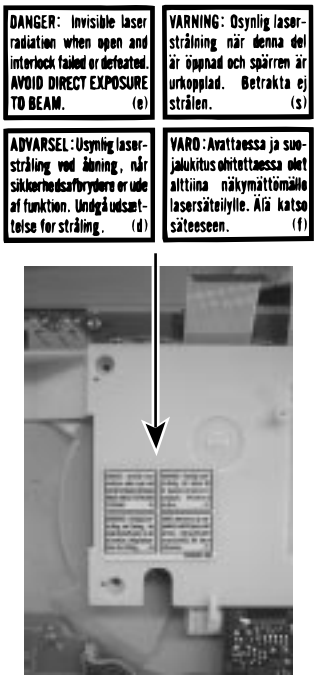
VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen.

ADVARSEL : Usynlig laserstråling ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

ADVARSEL : Usynlig laserstråling ved åpning,når sikkerhetsbryteren er avslott. unngå utsettelse for stråling.

REPRODUCTION AND POSITION OF LABELS

WARNING LABEL



Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

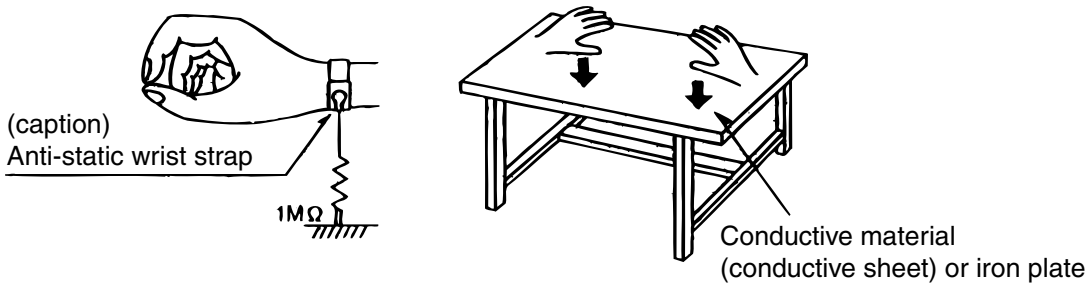
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Dismantling and assembling the traverse unit

Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

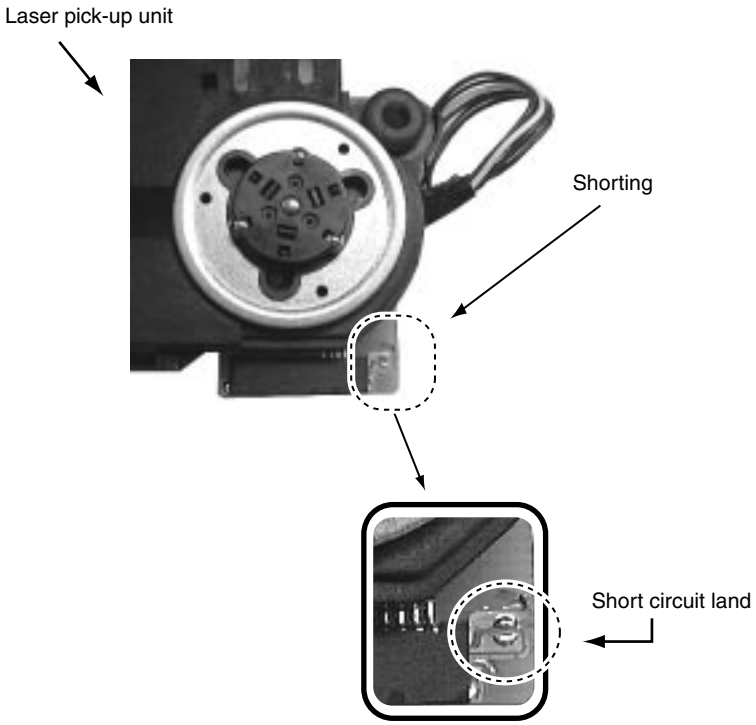
1. Do not touch the area around the laser diode and actuator.

2. Do not check the laser diode using a tester, as the diode may easily be destroyed.

3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.
Recommended soldering iron: HAKKO ESD-compatible product

4. Solder the land on the optical pickup's flexible cable.
- Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
- Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.

KSM-770ABA



Disassembly method

<Main body>

■Removing the CD door (See Fig.1)

1. Remove the four screws **A** attaching the CD door on the upper side of the body.

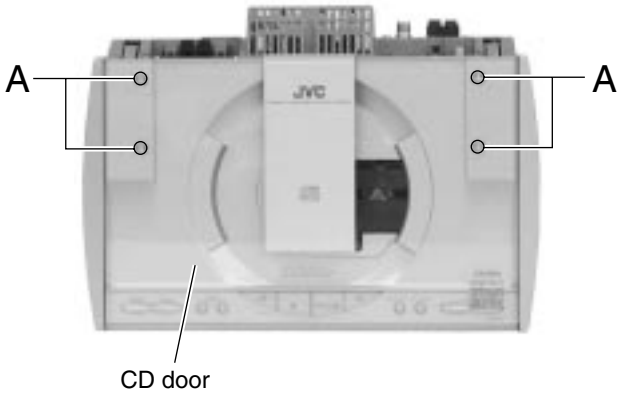


Fig.1

■Removing the rear cover (See Fig.2)

・ Piro to performing the following procedure, remove the CD door.

1. Remove the ten screws **B** and the five screws **C** attaching the rear cover on the back of the body.

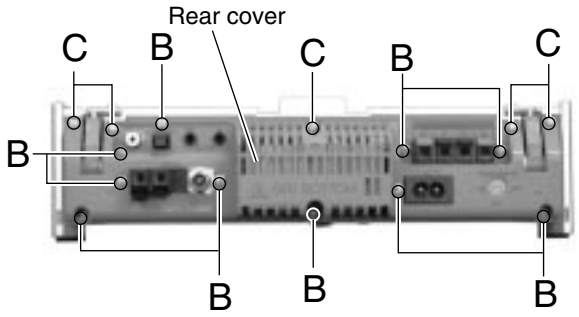


Fig.2

■Removing the right and left covers (See Fig.3)

・ Prior to performing the following procedure, remove the CD door, the rear cover.

1. Remove the four screws **D** attaching the side covers on the bottom of the body.

2. Move the left cover backward and remove outward. Also remove the right cover in the same way.

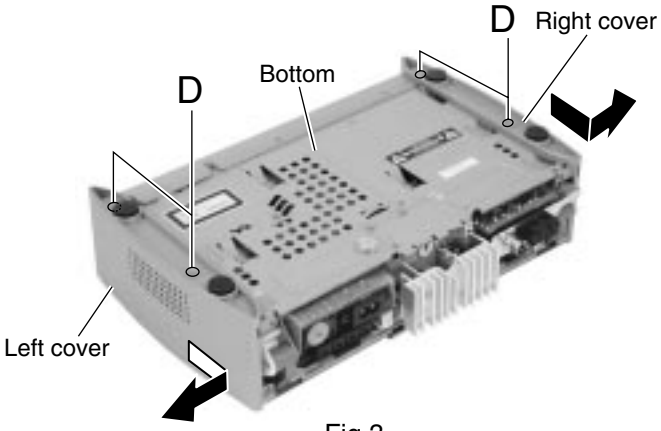


Fig.3

■Removing the front panel assembly (See Fig.4 to 6)

・Prior to performing the following procedure, remove the CD door, the rear cover and the side covers.

1. Remove the three screws **E** on the bottom of the body.

2. Release two joints **a** and two joints **b** on both sides of the body using a screwdriver and remove the front panel assembly toward the front.

   If necessary, remove the screw **F** which retains the wire extending from the front panel assembly.

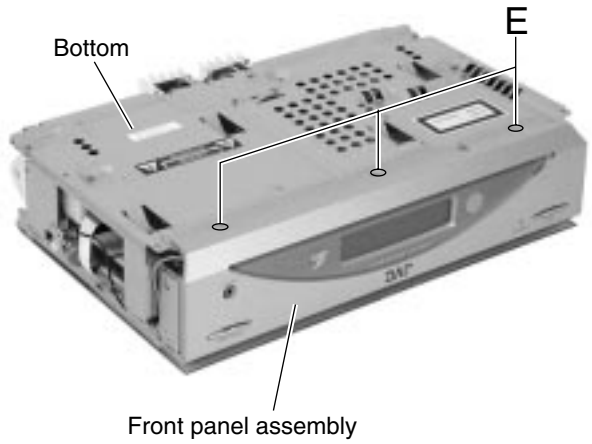


Fig.4

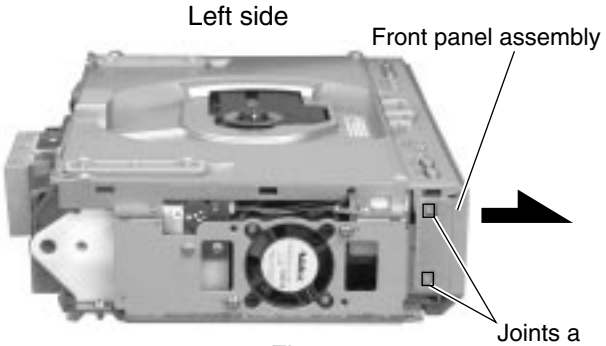


Fig.5

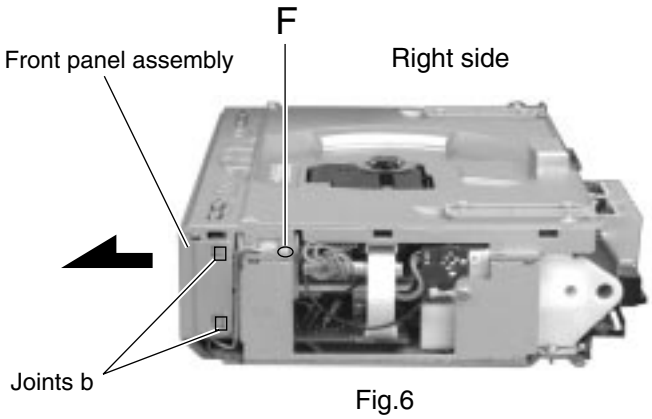


Fig.6

■Removing the CD mechanism base assembly (See Fig.7 to 14)

・Prior to performing the following procedure, remove the CD door, the rear cover, the side covers and the front panel assembly.

1. Disconnect the card wire from connector CN104 and CN105 of the main board in the front part of the body. Disconnect the card wire from CN101 of the main board on the right side, and the wire from CN705 of the CD mechanism base assembly respectively.

2. Remove the four screws **F** attaching the CD mechanism base assembly on the upper side of the body. Remove the screw **I** attaching the earth terminal on the right side.

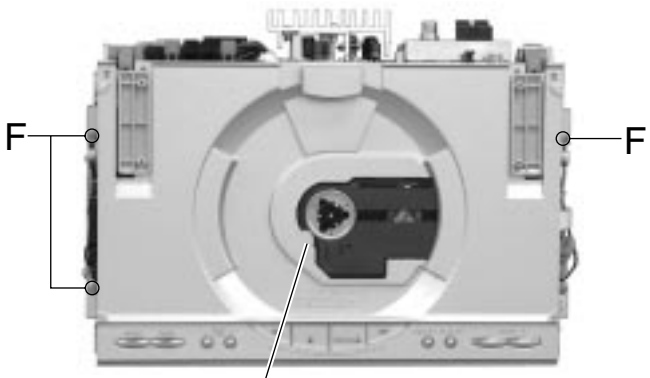


Fig.7

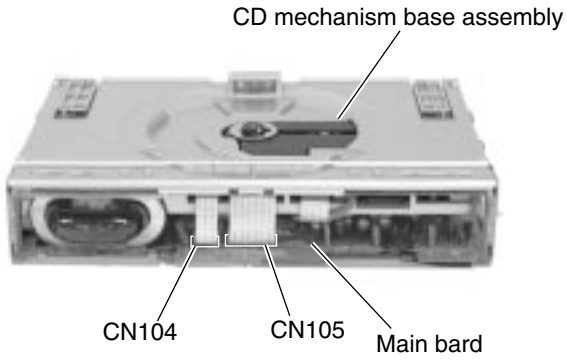


Fig.8

3. Remove the screw **G** attaching the heat sink board on the back of the body. Disconnect the wire from connector CN301 and pull the heat sink board fully outward.

4. Raise the right and left door arms by turning the gear **a** in the rear of the heat sink board.

5. After the CD mechanism base assembly is detached from the door arms, pull the CD mechanism base assembly toward the front and disconnect the wire from connector CN804 on the left side of the door arm board.

6. Pull out the CD mechanism base assembly toward the front.

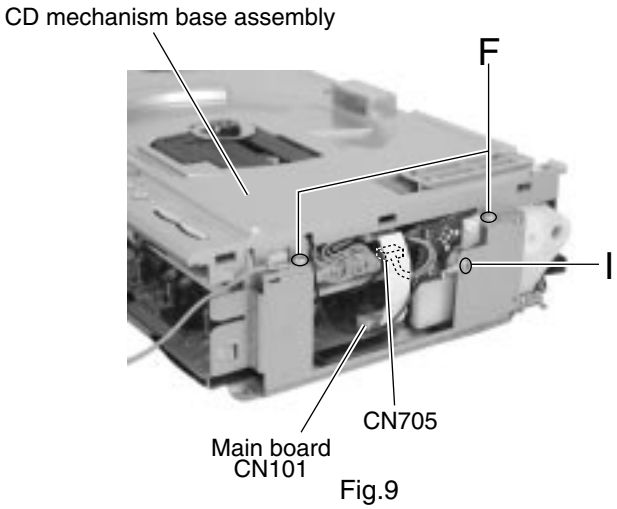


Fig.9

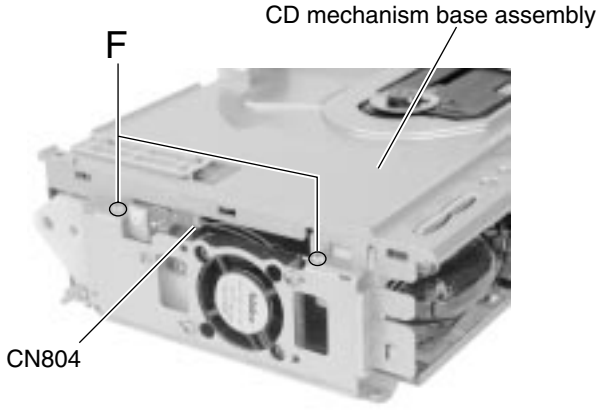


Fig.10

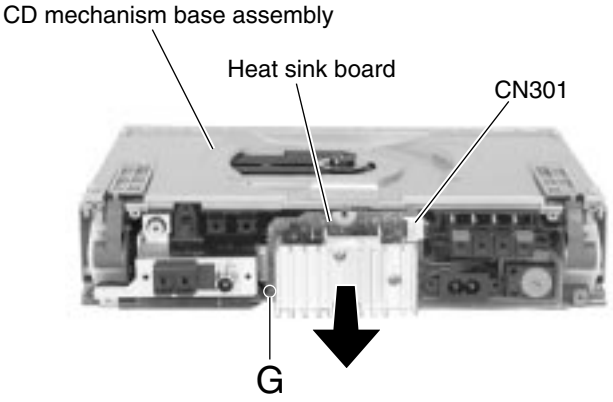


Fig.11

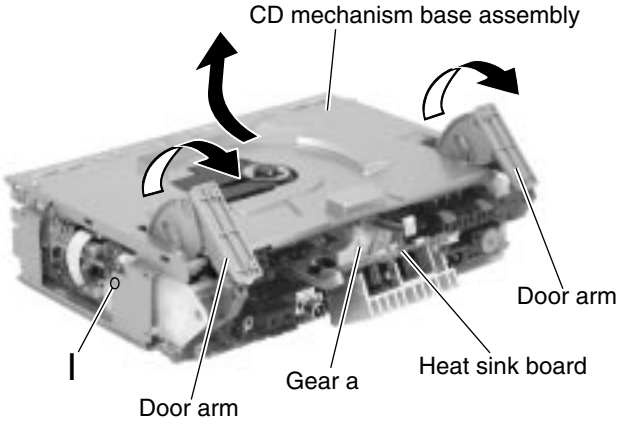


Fig.12

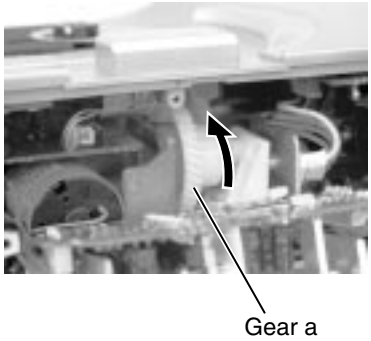


Fig.13

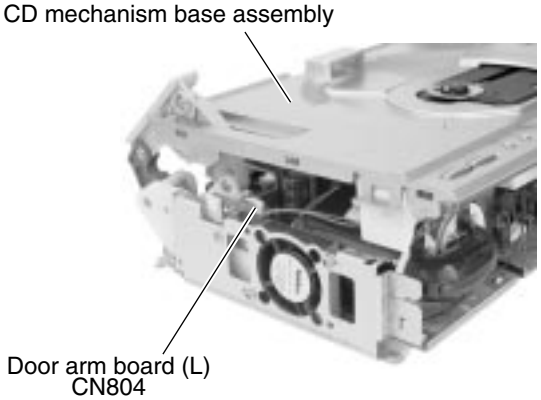


Fig.14

■Removing the door arm assembly / the door arm board (R) and (L) (See Fig.15 to 20)

・ Prior to performing the following procedure, remove the rear cover, the side covers, the front panel assembly and the CD mechanism base assembly.

1. In case that the upper parts of the door arms attached to the CD door are not level, let down them to the level position by turning the gear **a** in the direction of the arrow.

ATTENTION: When the door arms incline, the door arm assembly and the door arm board (R) and (L) may not be removed.

2. Remove the four screws **H** on the upper side and the one screw **I** on the left side of the body.

3. Remove the four screws **J** attaching the door arm board (L) and (R) on both sides of the door arm assembly.

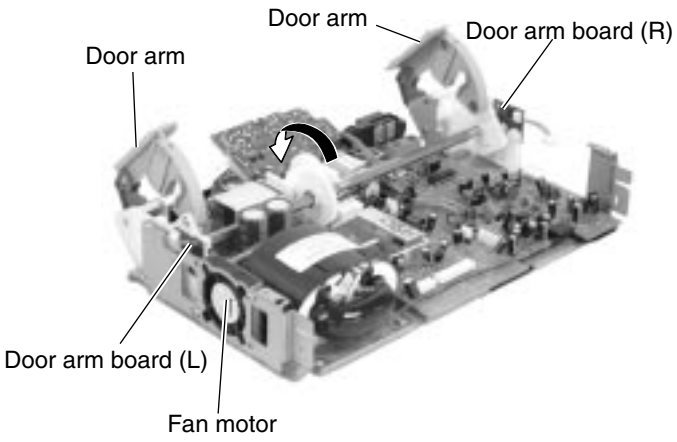


Fig.15

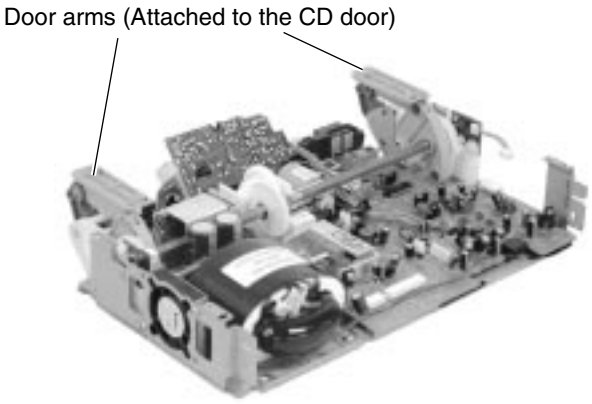


Fig.16

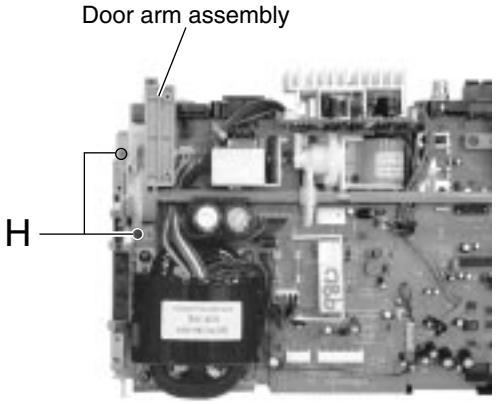


Fig.17

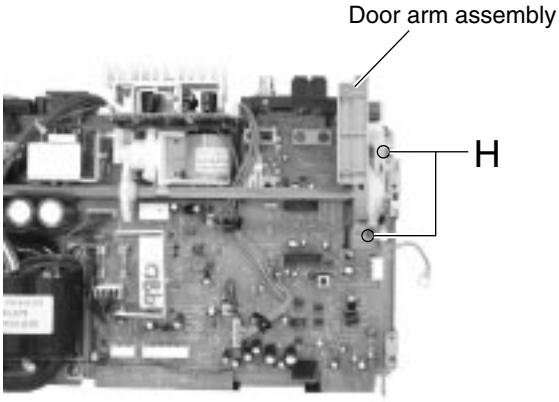


Fig.18

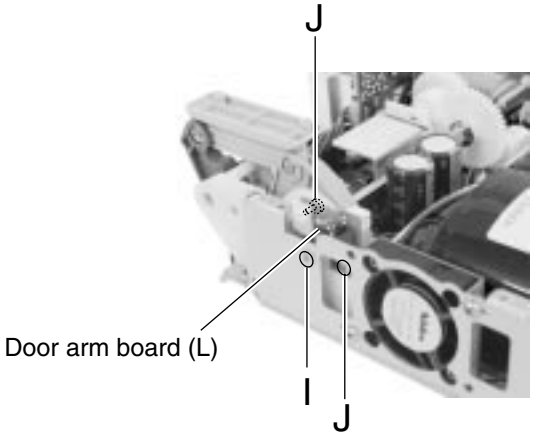


Fig.19

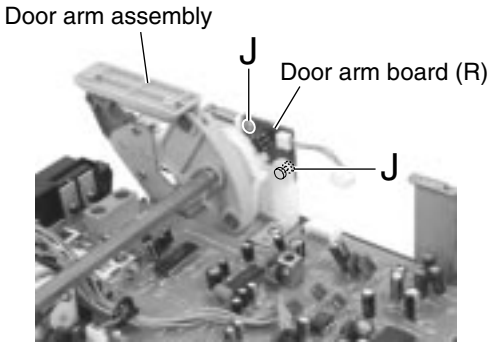


Fig.20

■Removing the power amplifier board (See Fig.21 and 22)

・ Prior to performing the following procedure, remove the CD mechanism base assembly.

1. Disconnect the wires from connector CN102 and CN193 on the main board and release them from the cord stopper respectively.

2. Remove the two screws **K** and the two screws **L** attaching the heat sink and the power amplifier board.

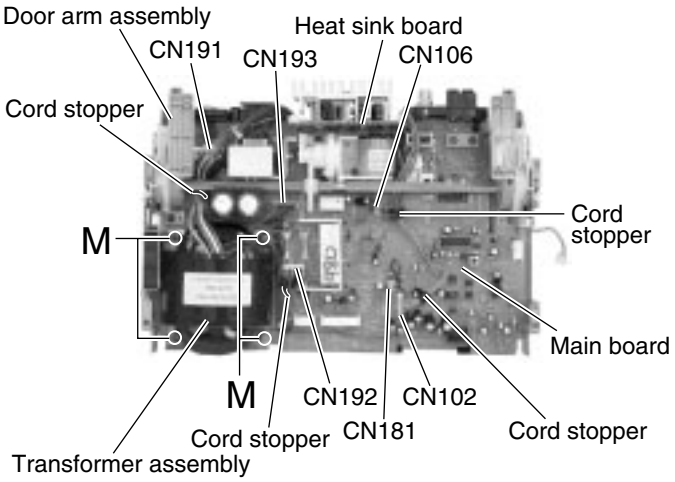


Fig.21

■Removing the transformer assembly (See Fig.21)

・ Prior to performing the following procedure, remove the CD mechanism base assembly.

1. Disconnect the wires from connector CN191 and CN192 on the main board and release them from the cord stopper respectively.

2. Remove the four screws **M** attaching the transformer assembly.

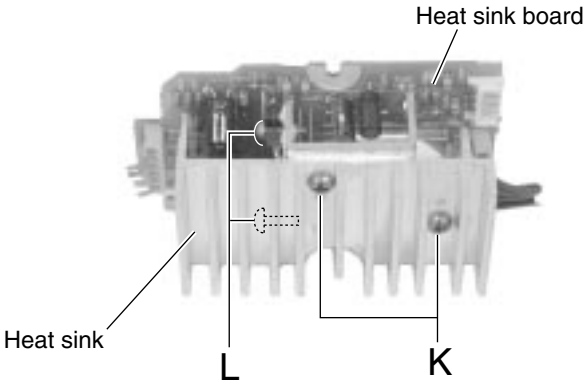


Fig.22

■Removing the gear motor assembly (See Fig.23 and 24)

・ Prior to performing the following procedure, remove the CD mechanism base assembly and the door arm assembly.

1. Disconnect the wires from connector CN106 on the main board and release it from the cord stopper.

2. Remove the three screws **N** attaching the gear motor assembly. Remove the gear motor assembly with the gear motor stopper.

3. Remove the belt from the gear motor assembly.

4. Remove the two screws **O** from the gear motor assembly.

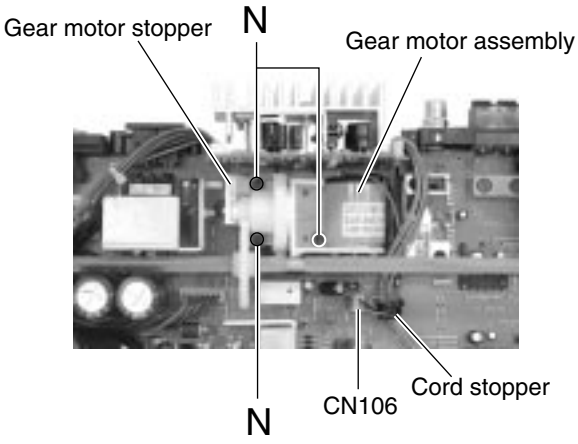


Fig.23

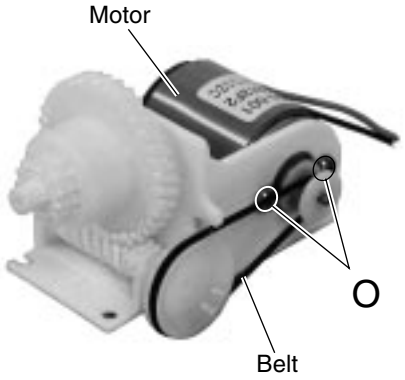


Fig.24

■Removing the fan motor assembly (See Fig.25 and 26)

・Prior to performing the following procedure, remove the CD mechanism base assembly.

1. Disconnect the wires from connector CN181 on the main board.

2. Remove the two screws **P** on the left side of the body. Move the fan motor assembly upward to remove it from the base chassis.

3. Remove the two screws **Q** and the fan motor from the fan bracket.

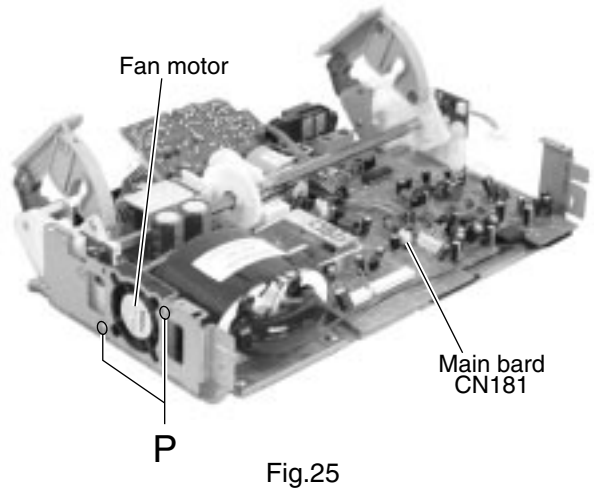


Fig.25

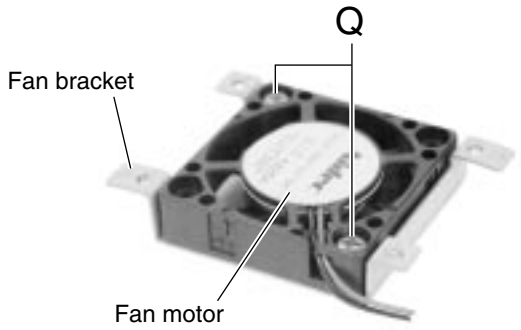


Fig.26

■Removing the main board (See Fig.27)

・Prior to performing the following procedure, remove the CD mechanism base assembly and the door arm assembly.

・To facilitate operation process, remove the gear motor assembly before performing the following procedure.

1. Disconnect the wires from connector CN102, CN106, CN191, CN192, CN193 and CN181 on the main board.

2. Remove the five screws **R** attaching the main board with the cord clamp.

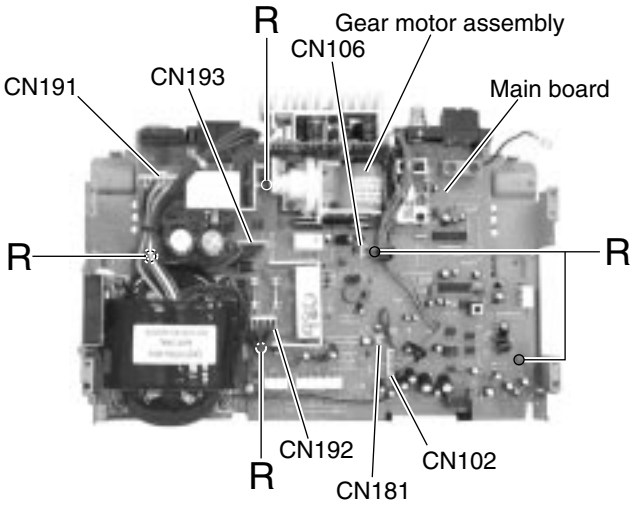


Fig.27

<Front panel assembly>

■Removing the front panel board (See Fig.28)

・Prior to performing the following procedure, remove the front panel assembly.

1. Remove the seven screws **S** attaching the front panel board inside the front panel assembly.

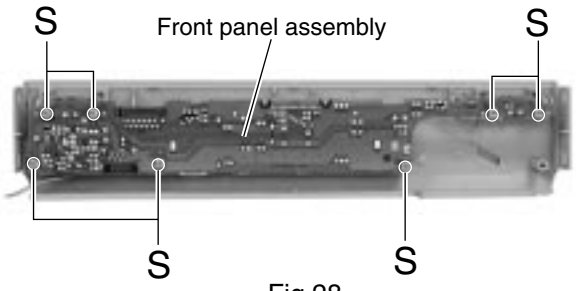


Fig.28

<CD mechanism base assembly>

・ Prior to performing the following procedure, remove the CD mechanism base assembly.

■Removing the speaker terminal board (See Fig.29)

1. Remove the screws **T** attaching the speaker terminal board on the underside of the CD mechanism base assembly.

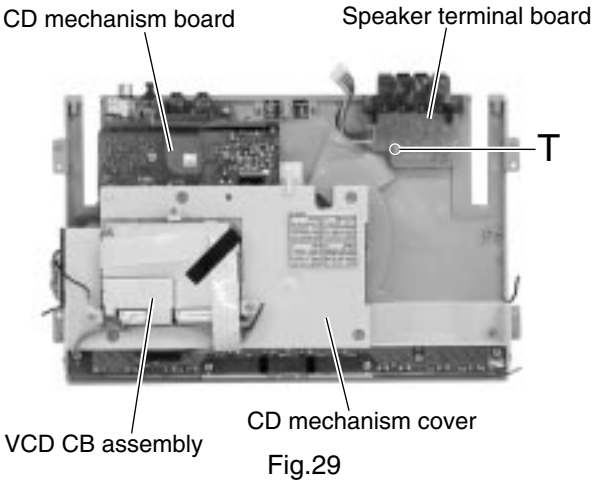


Fig.29

■Removing the VCD CB assembly (See Fig.30 to 33)

1. Disconnect the card wire from connector CN711 on the CD mechanism board attached to the CD mechanism base.

2. Disconnect the wires from connector CN102 and CN103 on the VCD CB assembly.

3. Unjoint the six joints (f) with the VCD shield (L) and the VCD shield (U). Remove the VCD shield (L) in the direction of the arrow.

4. Remove the VCD CB assembly from the VCD shield (L).

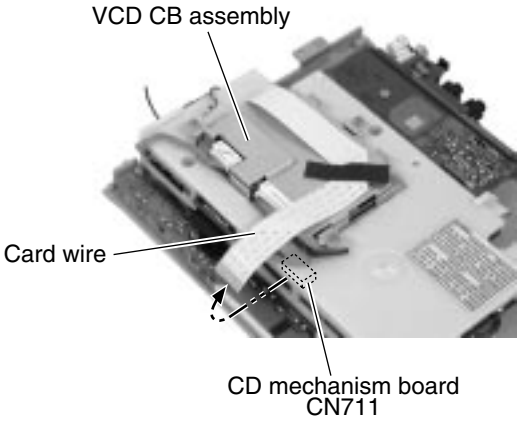


Fig.30

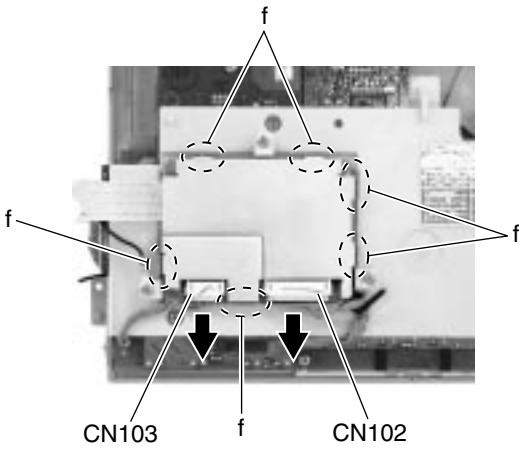


Fig.31

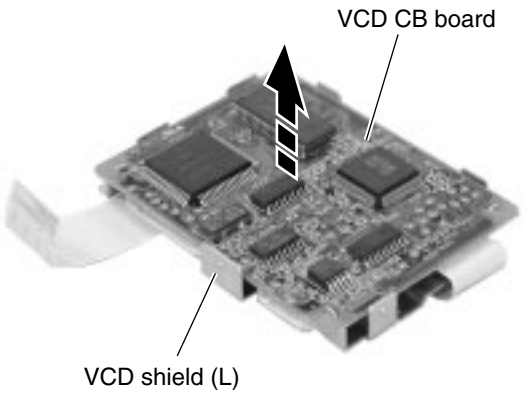


Fig.33

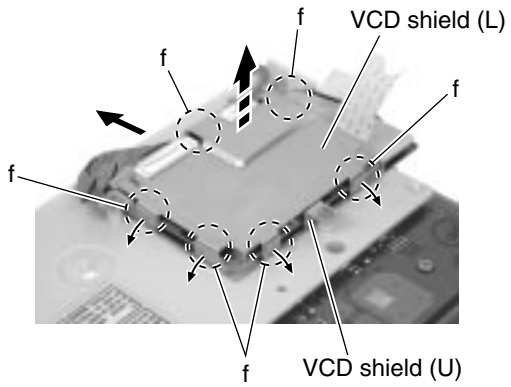


Fig.32

■Removing the CD mechanism board / mechanism assembly (See Fig.34 to 38)

・ Prior to performing the following procedure, remove the VCD CB assembly.

1. Turn over the CD mechanism assembly and remove the screw **X** which retains the wire extending from the CD mechanism board.

2. Remove the seven screws **U** attaching the CD mechanism cover and the CD mechanism board.

3. Disconnect the wire from connector CN703 and CN706 on the CD mechanism board respectively.

4. Turn back the CD mechanism assembly and detach the CD mechanism cover while pulling the CD mechanism assembly outward to release the two joint tabs marked **c**.

5. Disconnect the card wire from the connector of the CD mechanism assembly inside the CD mechanism cover. Disconnect the wire from CN605 on the CD mechanism board. Pull the CD mechanism assembly out of the three shaft of the CD mechanism cover.

ATTENTION: When reassembling, confirm that the cushion of the CD mechanism assembly is reattached to the three shafts.

6. Remove the CD mechanism board from the CD mechanism cover.

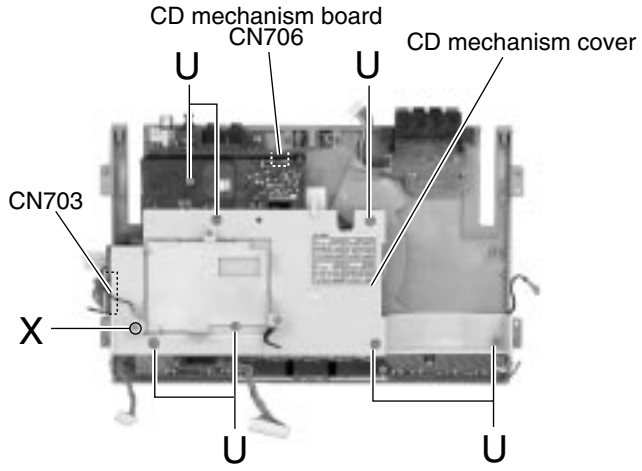


Fig.34

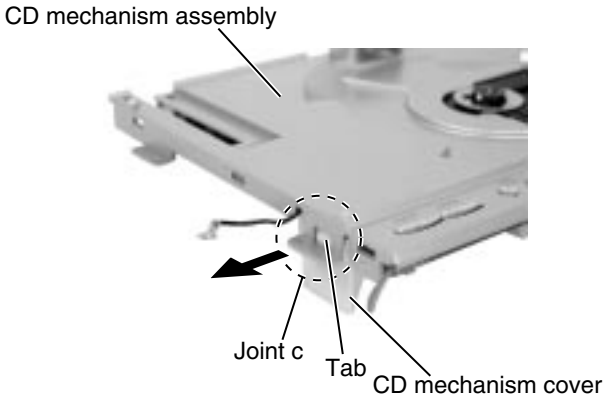


Fig.35

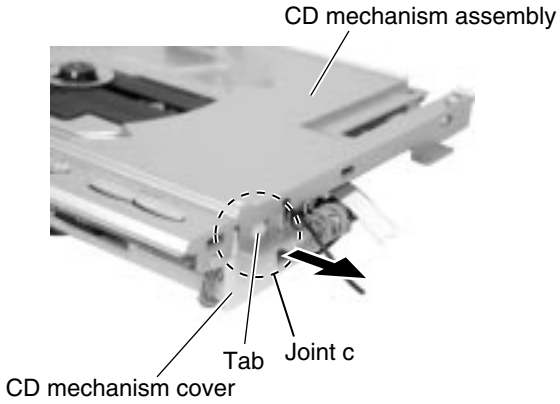


Fig.36

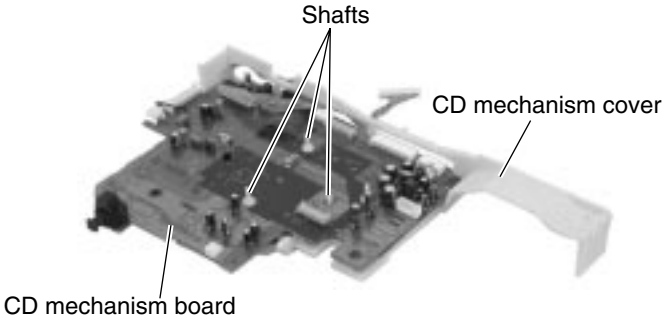


Fig.38

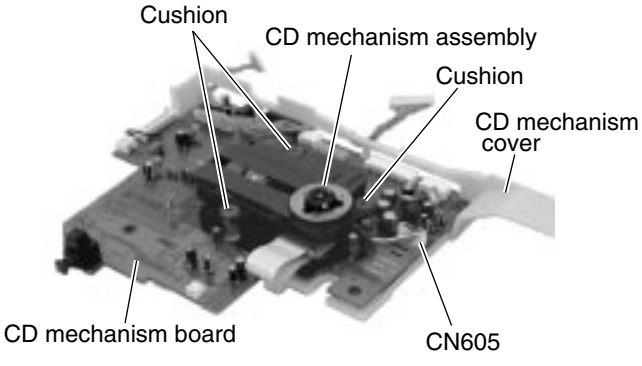


Fig.37

■Removing the jack board (See Fig.39)

・ Prior to performing following procedure, remove the CD mechanism board.

1. Disconnect the wire from connector CN502 on the jack board.
2. Remove the two screws **V** attaching the jack board.

■Removing the switch board (See Fig.39)

・ Prior to performing following procedure, remove the CD mechanism board.

1. Disconnect the wire from connector CN502 on the jack board.
2. Remove the six screws **W** attaching the switch board.

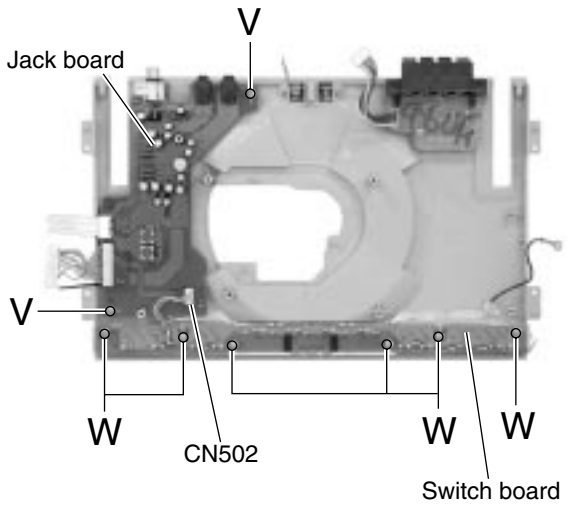


Fig.39

■Removing the LED board (See Fig.40 and 41)

1. Disconnect the wire from connector CN706 on the CD mechanism board on the underside of the CD mechanism base assembly.
2. Push inward the two tabs **d** attaching the LED board case and release them.
3. Pull out the LED board from the LED board case.

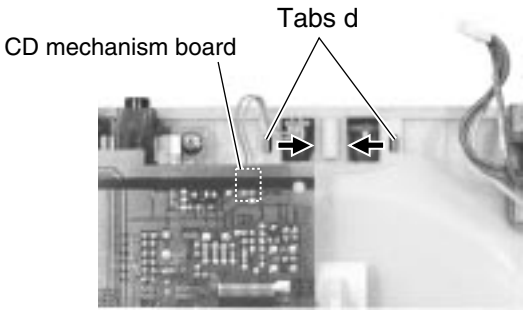


Fig.40

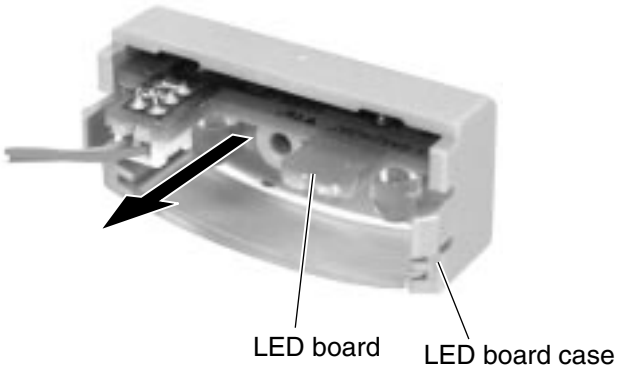


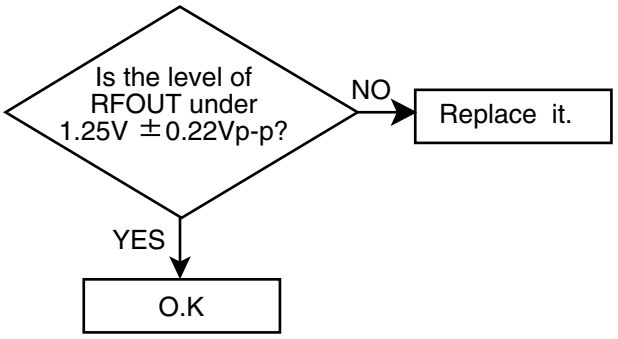
Fig.41

Maintenance of laser pickup

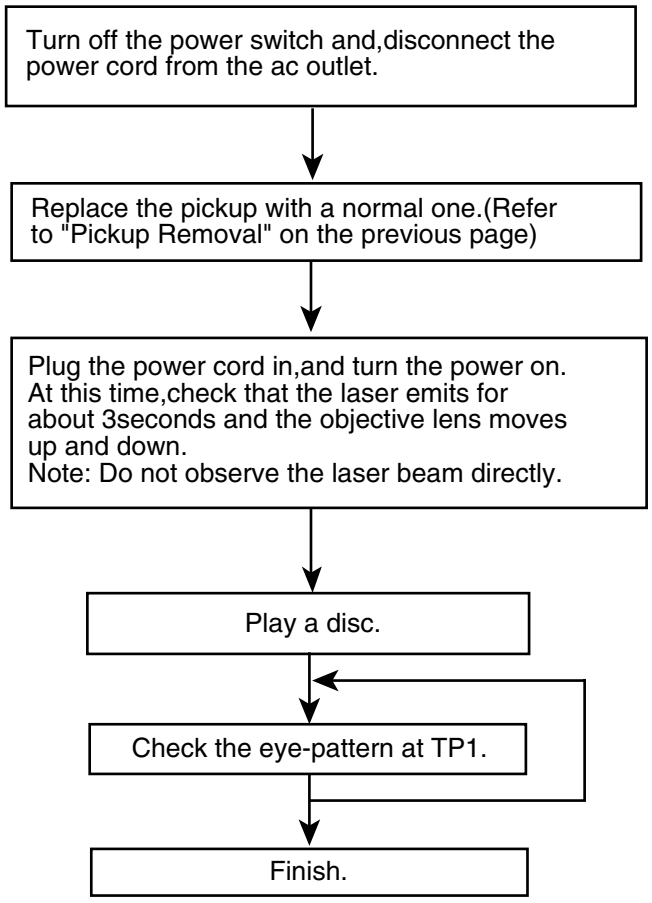
(1) Cleaning the pick up lens
Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.

(2) Life of the laser diode
When the life of the laser diode has expired, the following symptoms will appear.

1. The level of RF output (EFM output:amplitude of eye pattern) will below.

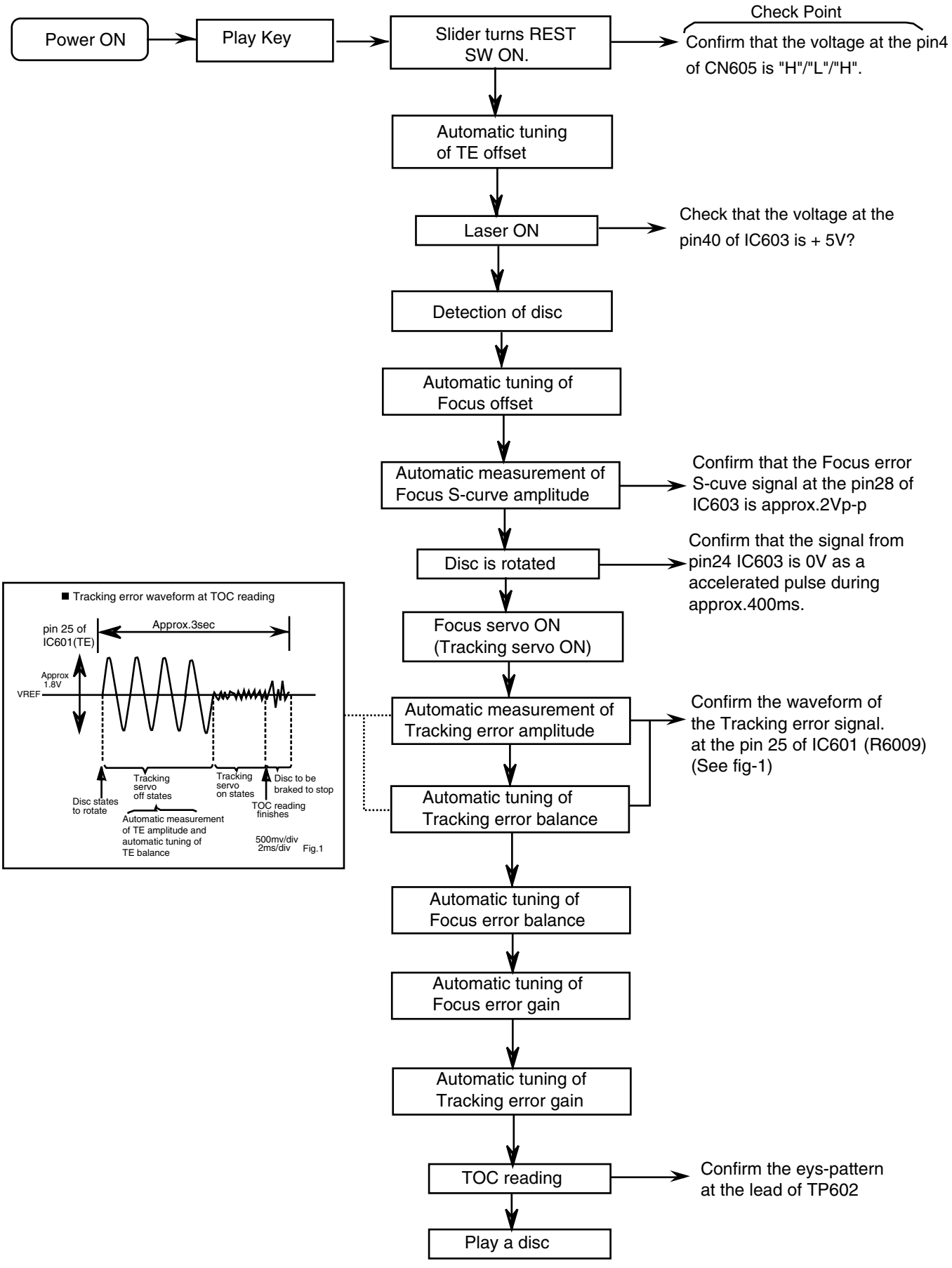


Replacement of laser pickup



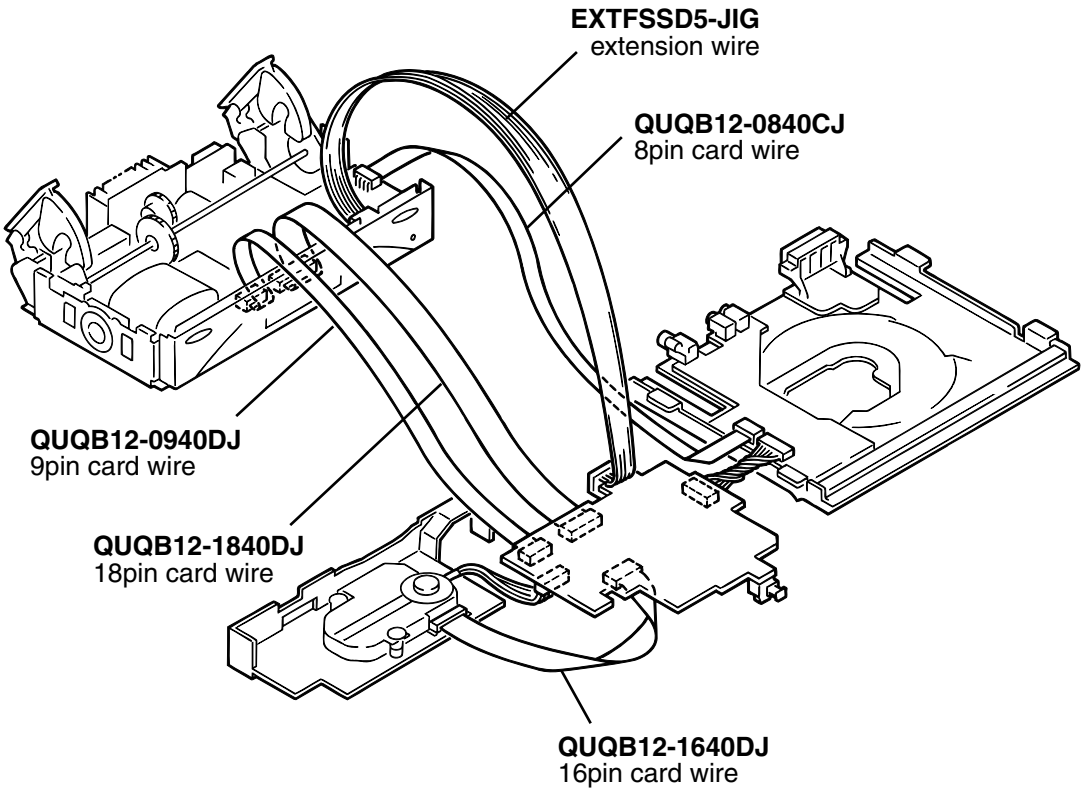
(3) Semi-fixed resistor on the APC PC board The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power.Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.
If the laser power is lower than the specified value,the laser diode is almost worn out, and the laser pickup should be replaced.
If the semi-fixed resistor is adjusted while the pickup is functioning normally,the laser pickup may be damaged due to excessive current.

Flow of functional operation until TOC read



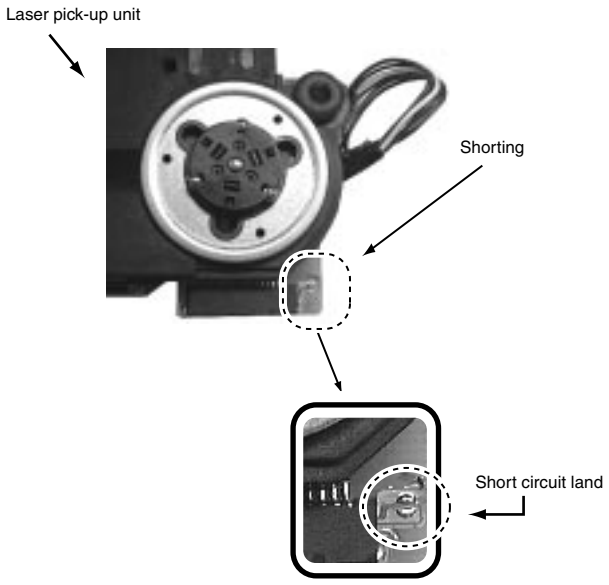
Method of connecting treatment device wire

When the KSM-770ABA mechanism is used, the expansion cable is used as follows.



First short-circuit the pickup circuit before removing the pickup.Then carry out the replacement.
Refer to "Dismantling and assembling the traverse unit" on page 1-5.

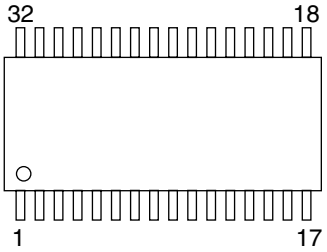
KSM-770ABA



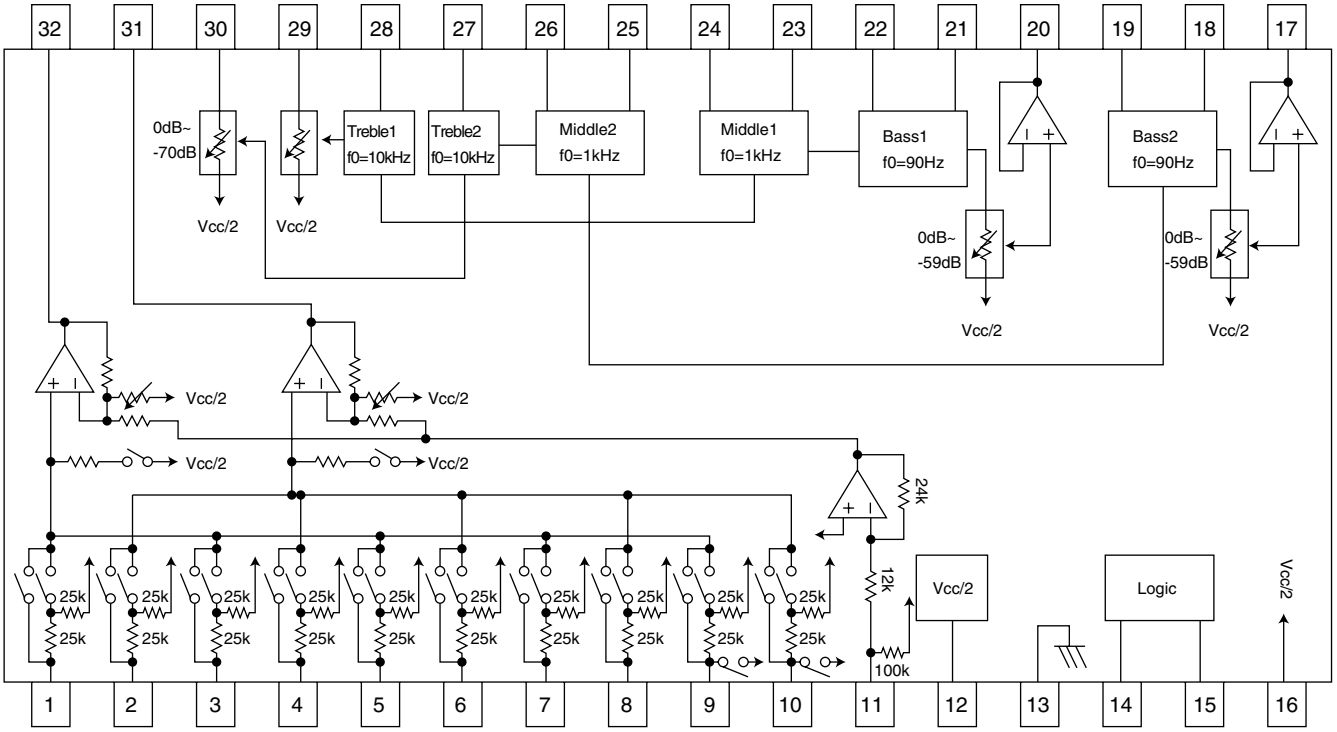
Description of major ICs

■BD3861FS-X (IC501) : Audio sound control

1. Pin layout



2. Block diagram

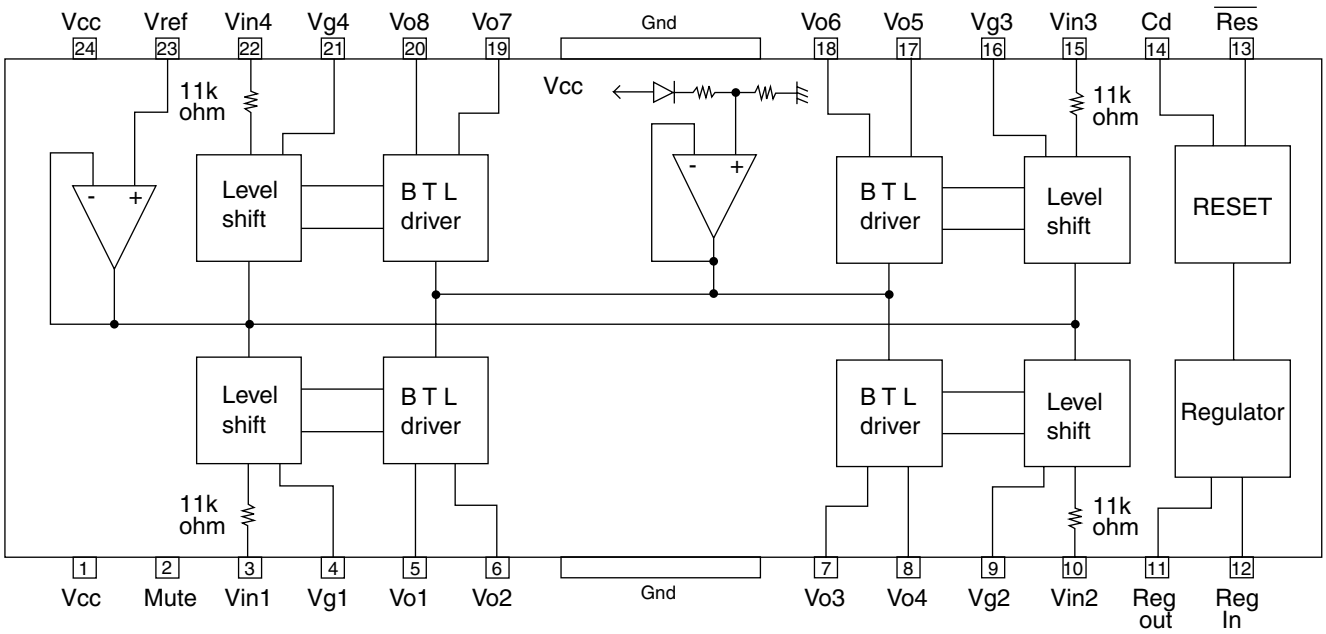


3. Pin function

Pin No.	Symbol	Function		Symbol	Function
1	A1	CH1 input pin A	17	OUT2	CH2 output pin
2	A2	CH2 input pin A	18	BASS21	CH2 bass filter setting pin
3	B1	CH1 input pin B	19	BASS22	CH2 bass filter setting pin
4	B2	CH2 input pin B	20	OUT1	CH1 output pin
5	C1	CH1 input pin C	21	BASS11	CH1 bass filter setting pin
6	C2	CH2 input pin C	22	BASS12	CH1 bass filter setting pin
7	D1	CH1 input pin D	23	MID11	CH1 middle filter setting pin
8	D2	CH2 input pin D	24	MID12	CH1 middle filter setting pin
9	E1	CH1 input pin E	25	MID21	CH2 middle filter setting pin
10	E2	CH2 input pin E	26	MID22	CH2 middle filter setting pin
11	MIC	Microphone input pin	27	TRE2	CH2 treble filter setting pin
12	FIL	Filter pin	28	TRE1	CH1 treble filter setting pin
13	GND	Ground pin	29	VOL1	CH1 input volume input pin
14	DATA	Serial data latch receiving pin	30	VOL2	CH2 input volume input pin
15	CLK	Serial clock receiving pin	31	GOUT2	CH2 input gain output pin
16	Vcc	Power supply pin	32	GOUT1	CH1 input gain output pin

■ LA6541-X(IC602) : Servo Driver

1. Pin Layout & Block Diagram

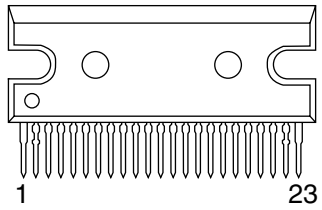


2. Pin functions

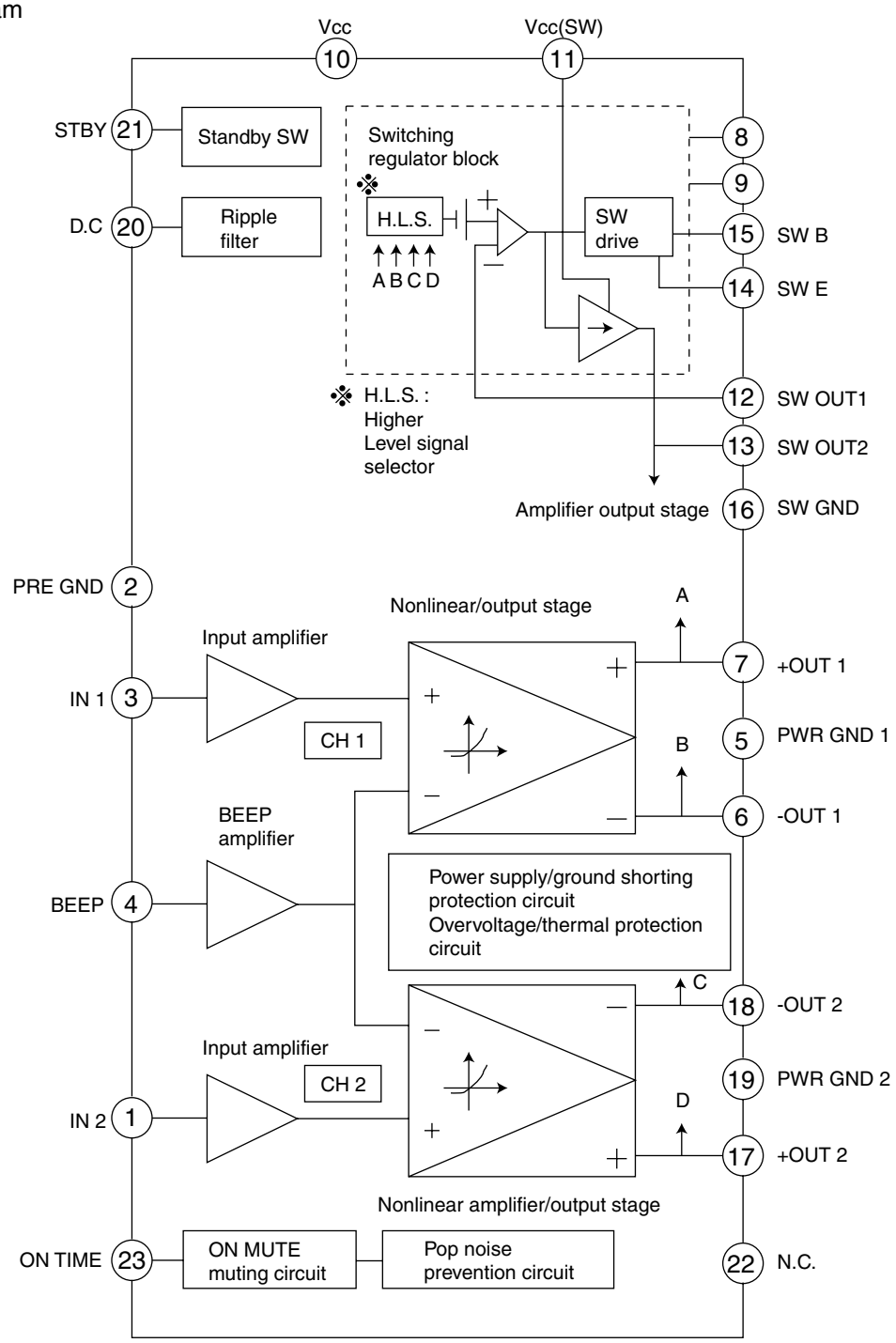
Pin No.	Symbol	Function
1	Vcc	Power supply (Shorted to pin 24)
2	Mute	All BTL amplifier outputs ON/OFF
3	Vin1	BTL AMP 1 input pin
4	Vg1	BTL AMP 1 input pin (For gain adjustment)
5	Vo1	BTL AMP 1 input pin (Non inverting side)
6	Vo2	BTL AMP 1 input pin (Inverting side)
7	Vo3	BTL AMP 2 input pin (Inverting side)
8	Vo4	BTL AMP 2 input pin (Non inverting side)
9	Vg2	BTL AMP 2 input pin (For gain adjustment)
10	Vin2	BTL AMP 2 input pin
11	Reg Out	External transistor collector (PNP) connection. 5V power supply output
12	Reg In	External transistor (PNP) base connection
13	Res	Reset output
14	Cd	Reset output delay time setting (Capacitor connected externally)
15	Vin3	BTL AMP 3 input pin
16	Vg3	BTL AMP 3 input pin (For gain adjustment)
17	Vo5	BTL AMP 3 output pin (Non inverting side)
18	Vo6	BTL AMP 3 output pin (Inverting side)
19	Vo7	BTL AMP 4 output pin (Inverting side)
20	Vo8	BTL AMP 4 output pin (Non inverting side)
21	Vg4	BTL AMP 4 output pin (For gain adjustment)
22	Vin4	BTL AMP 4 output pin
23	Vref	Level shift circuit's reference voltage application
24	Vcc	Power supply (Shorted to pin 1)

■ LA4905 (IC301) : 2ch BTL power IC

1. Pinlayput

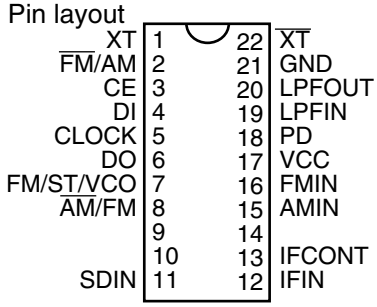


2. Block diagram

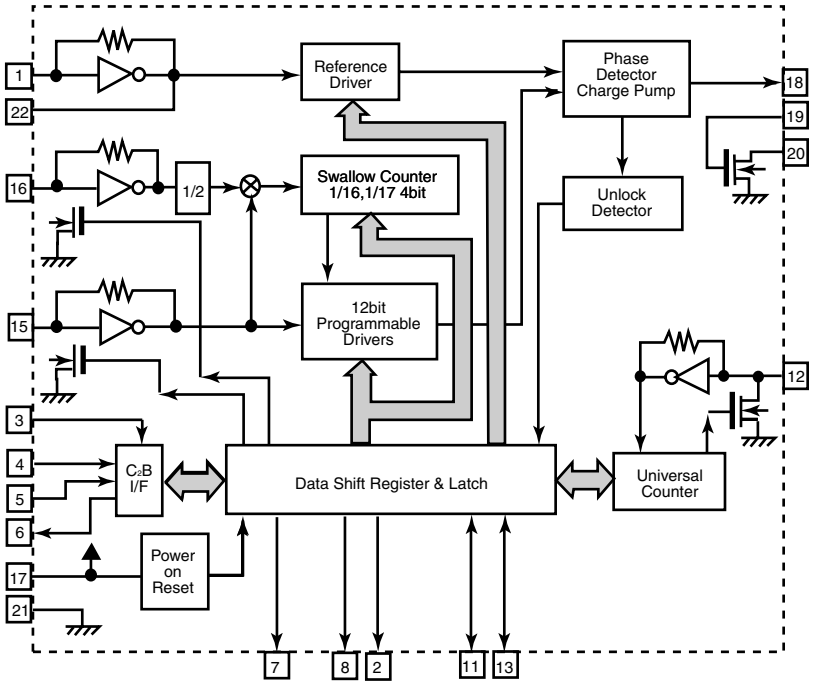


■LC72136N (IC2) : PLL Frequency synthesizer

1. Pin layout



2. Block

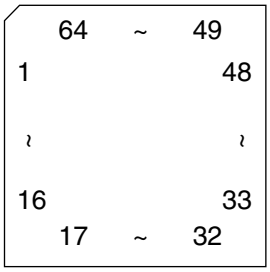


3. Function

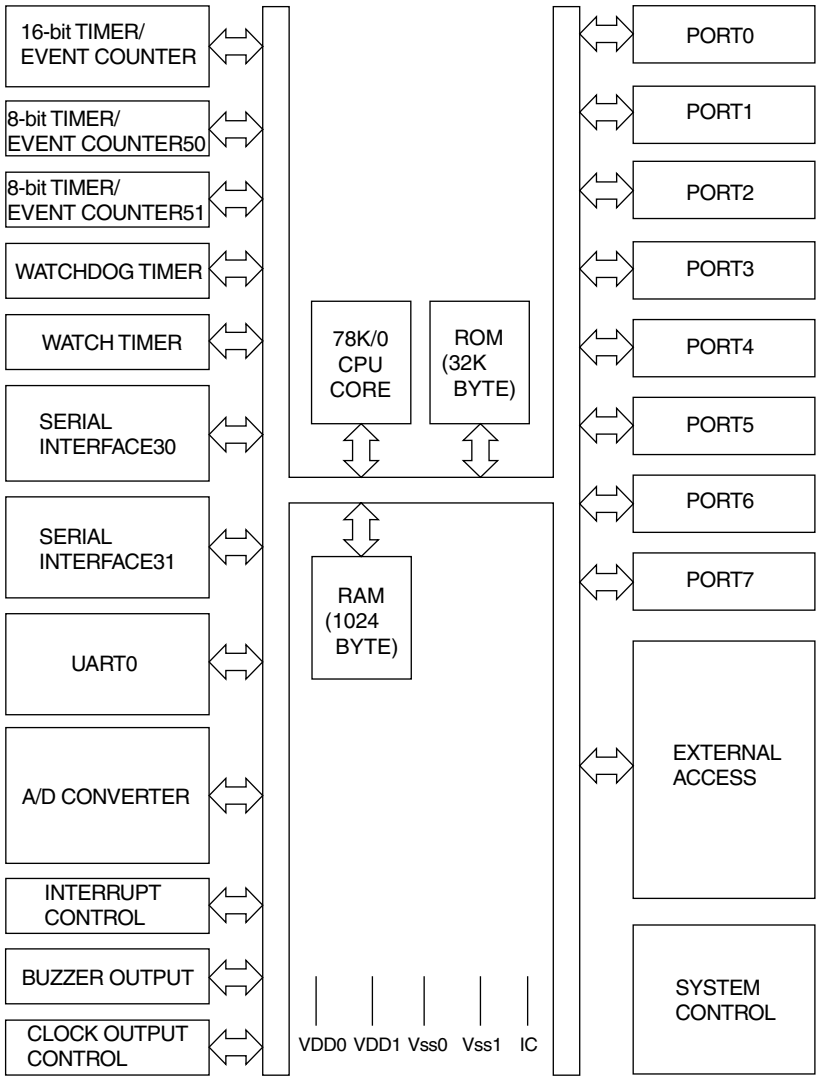
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	XT	I	X'tal oscillator connect (75kHz)	12	IFIN	I	IF counter signal input
2	$\overline{FM}$/AM	O	LOW:FM mode	13	IFCONT	O	IF signal output
3	CE	I	When data output/input for 4pin(input) and 6pin(output): H	14		-	Not use
4	DI	I	Input for receive the serial data from controller	15	AMIN	I	AM Local OSC signal output
5	CLOCK	I	Sync signal input use	16	FMIN	I	FM Local OSC signal input
6	DO	O	Data output for Controller Output port	17	VCC	-	Power suplly(VDD=4.5-5.5V) When power ON:Reset circuit move
7	FM/ST/VCO	O	"Low": MW mode	18	PD	O	PLL charge pump output(H: Local OSC frequency Height than Reference frequency. L: Low Agreement: Height impedance)
8	$\overline{AM}$/FM	O	Open state after the power on reset	19	LPFIN	I	Input for active lowpassfilter of PLL
9	LW	I/O	Input/output port	20	LPFOUT	O	Output for active lowpassfilter of PLL
10	MW	I/O	Input/output port	21	GND	-	Connected to GND
11	SDIN	I/O	Data input/output	22	$\overline{XT}$	I	X'tal oscillator(75KHz)

■ UPD780024AGKB09 (IC701) : CPU

1. Pin layout



2. Block diagram



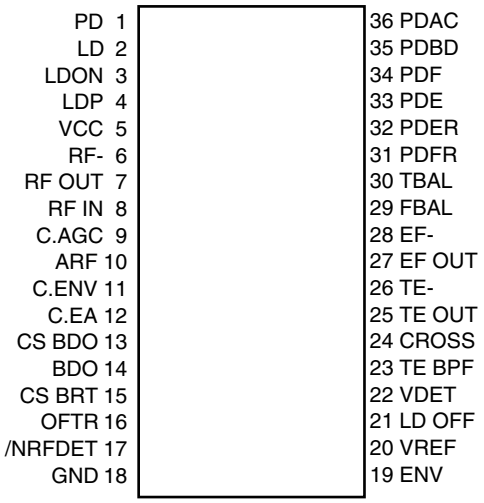
3. Pin function

UPD780024AGKB09

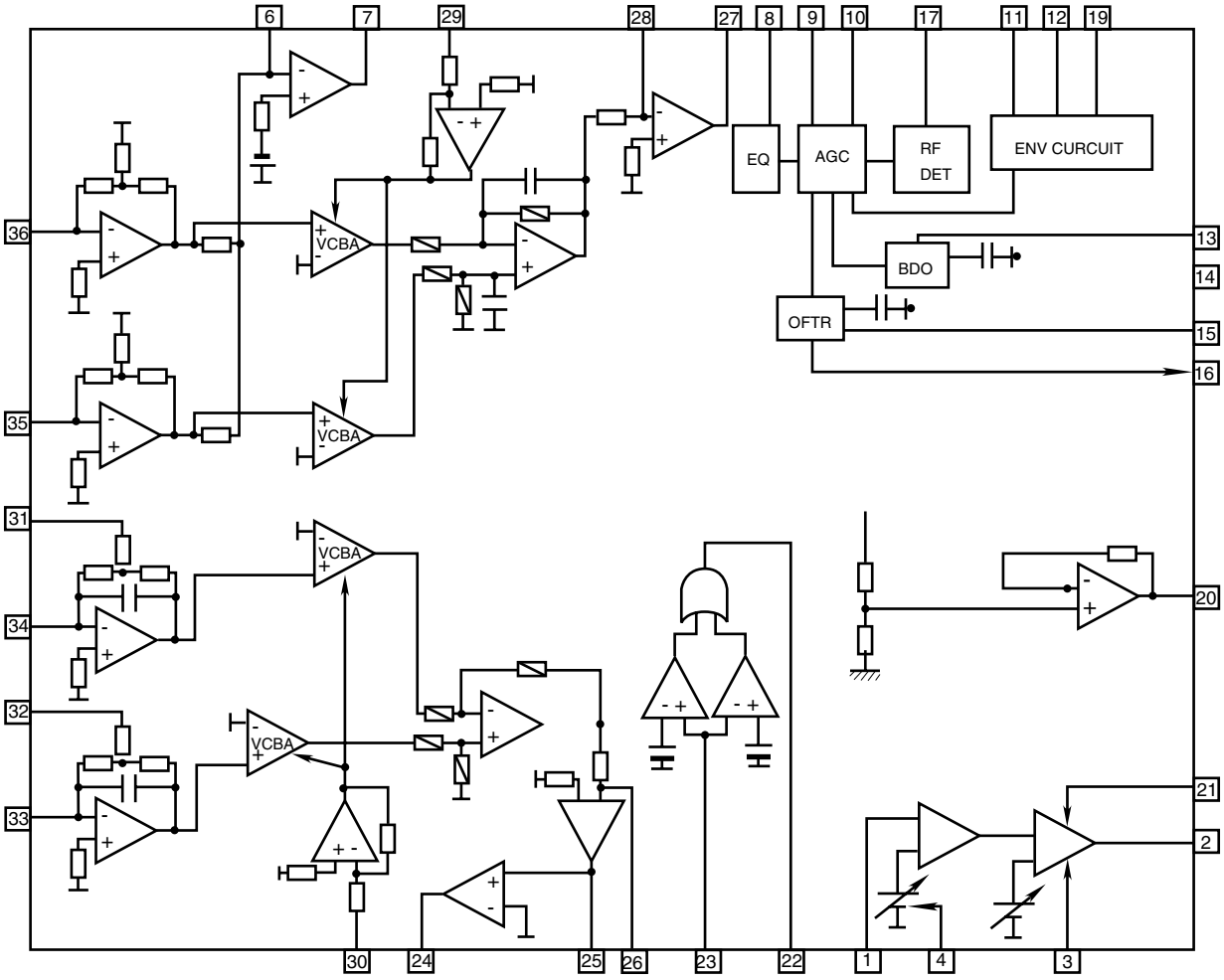
Pin No.	Symbol	I/O	Function
1	MT0	O	CD door motor control signal 0 output
2	MT1	O	CD door motor control signal 1 output
3	MTS	O	Motor speed control output (L:Normal, H:Slow)
4	BLCTL	O	Back light power supply control output
5	AHB	O	AHB ON/OFF control signal output (L:ON, H:OFF)
6	SMUTE	O	System mute control signal output
7	TUST	O	Tuner control strove output
8	CDLED	O	CD LED control signal output (L:OFF, H:ON)
9	VSS0	-	Ground at port section
10	VDD0	-	Power supply at port section
11	MPX	I	Stereo indicator control signal input (L:Stereo)
12	RDSDI	I	RDS data input
13	DRMUTE	O	Driver mute output
14	SCD	I	Voltage detection for safety of CD
15	TUDATA(I)	I	Tuner control data input
16	TUDATA(O)	O	Tuner control data output
17	TUCK	O	Tuner control clock output
18	SUBQ	I	CD control Q code input
19	XRST	O	CD control reset signal output
20	SQCK	O	CD control Q code clock signal output
21	MLD	O	CD control command load signal output
22	MDATA	O	CD control command data signal output
23	MCLK	O	CD control command clock signal output
24	VDD1	-	Power supply without port section
25	AVSS	-	Ground of A/D converter
26	STAT	I	CD control status signal input
27	REST	I	CD rest switch detection signal input
28	KEY1	I	Main body top section tact switch detection signal input
29	KEY2	I	Main body top section tact switch detection signal input
30	KEY3	I	Main body front section tact switch detection signal input
31	SAFETY	I	Voltage detection for safety
32	LDCK	I	CD door motor lock detection signal input
33	VERSION	I	Version detection
34	AVREF	I	Reference voltage input for A/D converter
35	AVDD	-	Analog power supply for A/D converter
36	RESET	I	System reset signal input
37	XT2	-	Sub clock
38	XT1	I	Sub clock signal input 32.768kHz
39	IC	I	Connect to VSS0 or VSS1
40	X2	-	Main clock
41	X1	I	Main clock signal input 4.19MHz
42	VSS1	-	Ground without port section
43	REM	I	Remote controller signal input
44	RDSCK	I	RDS clock signal input
45	XKILL	O	Sub clock OSC control signal output
46	BEAT	O	Main clock shift control signal output
47	BUP	I	Back up detection signal input
48	+BCTL	O	Power supply control at back up operating
49	VDATA	O	BD3861FS (VOL & FUNC IC) control data signal output
50	VCLK	O	BD3861FS (VOL & FUNC IC) control clock signal output
51	DOOR1	I	Cd door position detection switch input
52	DOOR2	I	CD door position detection switch input
53	DOOR3	I	CD door position detection switch input
54	LOMUTE	O	LINE OUT muting control signal output
55	RS	O	LCD driver control resistor select signal output
56	E	O	LCD driver control enable signal output
57	D84	O	LCD driver control data bus signal output
58	D85	O	LCD driver control data bus signal output
59	D86	O	LCD driver control data bus signal output
60	D87	O	LCD driver control data bus signal output
61	DIMMER	O	Back light DIMMER control signal output
62	POUT	O	Power supply control signal output for amp section
63	FTU	O	Power supply control signal output for TUNER function
64	FCD	O	Power supply control signal output for CD function

■ AN8806SB-W(IC601) :RF&SERVO AMP

1.Pin layout



2.Block diagram



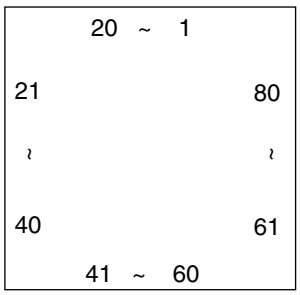
3. Pin function

AN8806SB-W

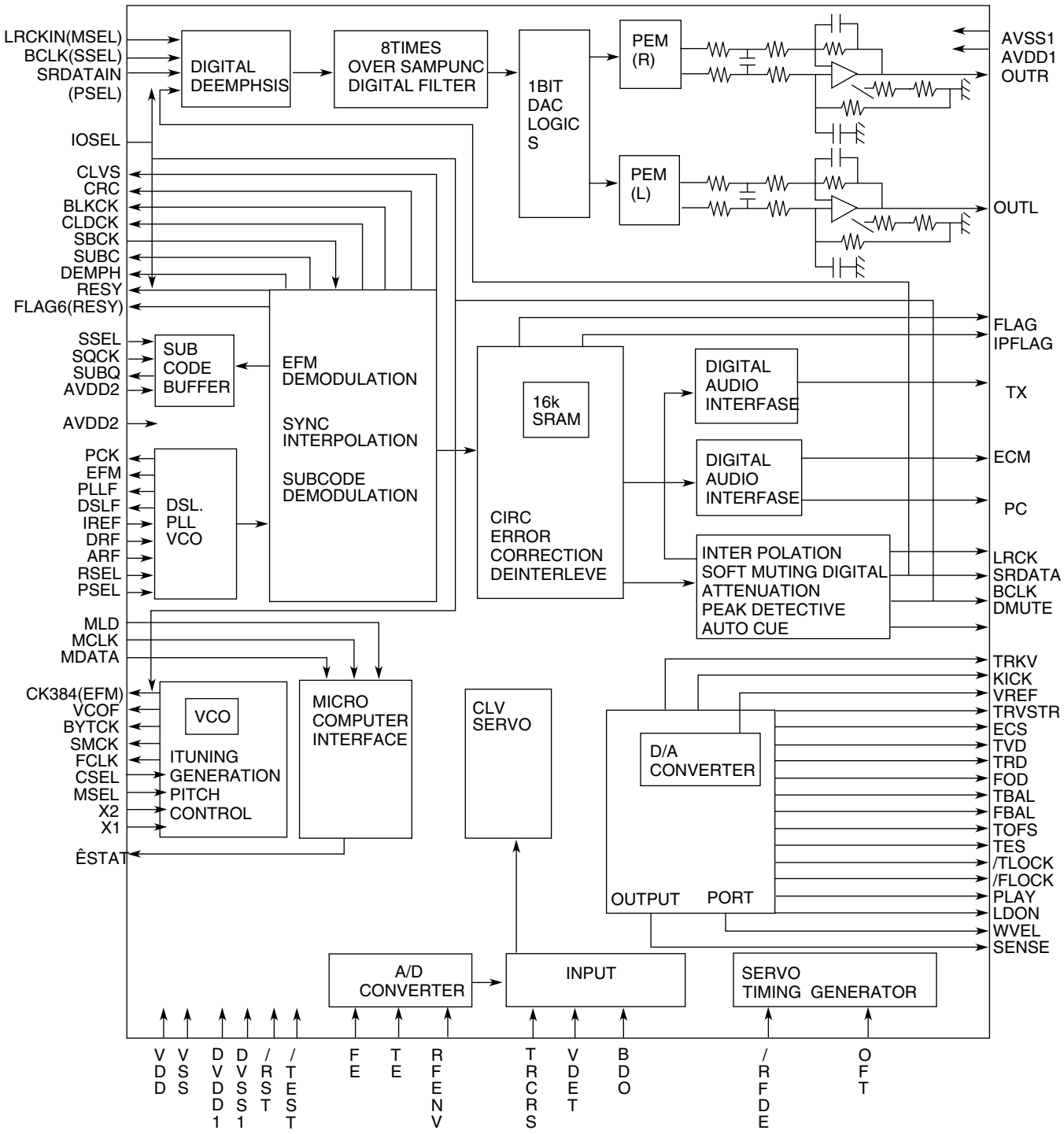
Pin No.	symbol	I/O	Function
1	PD	I	APC amp . Input terminal
2	LD	O	APC amp . Output terminal
3	LD ON	I	LD ON/OFF control terminal
4	LDP	--	Connect to GND
5	VCC	--	Power supply
6	RF-	I	RF amp . Reversing input terminal
7	RF OUT	O	RFamp . Output terminal
8	RF IN	I	AGC input terminal
9	C.AGC	I/O	AGC loop filter connection terminal
10	ARF	O	ARF output terminal
11	C.ENV	I/O	RF detection capacity connection terminal
12	C.EA	I/O	HPF-amp capacity connection terminal
13	CS BDO	I/O	Capacity connection terminal for RF discernment side envelope detection
14	BDO	O	BDO output terminal
15	CS BRT	I/O	Capacity connection terminal for RF discernment side envelope detection
16	OFTR	O	OFTR output terminal
17	/NRFDET	O	RFDET output terminal
18	GND	--	Connect to GND
19	ENV	O	3TENV output terminal
20	VREF	O	VREF output terminal
21	LD OFF	--	APC OFF control terminal
22	VDET	O	VDET output terminal
23	TE BPF	I	VDET input terminal
24	CROSS	O	CROSS output terminal
25	TE OUT	O	TE amp . Output terminal
26	TE-	I	FE amp . Reversing input terminal
27	FE OUT	O	FE amp . output terminal
28	FE-	I	FE amp . Reversing input terminal
29	FBAL	I	F.BAL control terminal
30	TBAL	I	T.BAL control terminal
31	PDFR	I/O	I-V amp conversion resistance adjustment terminal
32	PDER	I/O	I-V amp conversion resistance adjustment terminal
33	PDF	I	I-V amp input terminal
34	PDE	I	I-V amp input terminal
35	PD BD	I	I-V amp input terminal
36	PD AC	I	I-V amp input terminal

■MN35510(IC603):Digital servo & Digital signal processer

1. Terminal Layout



2.Block Diagram



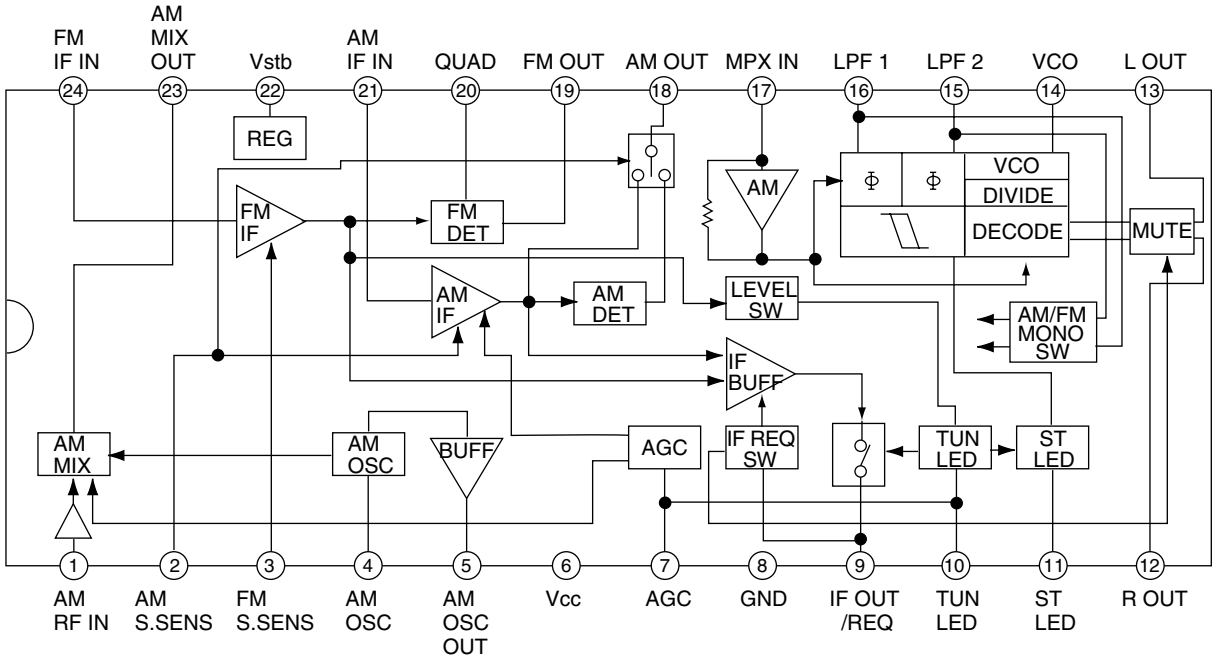
3. Description

MN35510

Pin No.	symbol	I/O	Description	Pin No.	symbol	I/O	Description
1	BCLK	O	Not used	41	TES	O	Tracking error shunt signal output(H:shunt)
2	LRCK	O	Not used	42	PLAY	—	Not used
3	SRDATA	O	Not used	43	WVEL	—	Not used
4	DVDD1	—	Power supply (Digital)	44	ARF	I	RF signal input
5	DVSS1	—	Connected to GND	45	IREF	I	Reference current input pin
6	TX	O	Digital audio interface output	46	DRF	I	Bias pin for DSL
7	MCLK	I	Micom command clock signal input (Data is latched at signal's rising point)	47	DSLF	I/O	Loop filter pin for DSL
8	MDATA	I	Micom command data input	48	PLLF	I/O	Loop filter pin for PLL
9	MLD	I	Micom command load signal input	49	VCOF	—	Not used
10	SENSE	O	Sence signal output	50	AVDD2	—	Power supply(Analog)
11	FLOCK	O	Focus lock signal output Active :Low	51	AVSS2	—	Connected to GND(Analog)
12	TLOCK	O	Tracking lock signal output Active :Low	52	EFM	—	Not used
13	BLKCK	O	sub-code - block - clock signal output	53	PCK	—	Not used
14	SQCK	I	Outside clock for sub-code Q resister input	54	PDO	—	Not used
15	SUBQ	O	Sub-code Q -code output	55	SUBC	—	Not used
16	DMUTE	—	Connected to GND	56	SBCK	—	Not used
17	STATUS	O	Status signal (CRC,CUE,CLVS,TTSTOP,ECLV,SQOK)	57	VSS	—	Connected to GND(for X'tal oscillation circuit)
18	RST	I	Reset signal input (L:Reset)	58	XI	I	Input of 16.9344MHz X'tal oscillation circuit
19	SMCK	—	Not used	59	X2	O	Output of X'tal oscillation circuit
20	PMCK	—	Not used	60	VDD	—	Power supply(for X'tal cscillation circuit)
21	TRV	O	Traverse enforced output	61	BYTCK	—	Not used
22	TVD	O	Traverse drive output	62	CLDCK	—	Not used
23	PC	—	Not used	63	FLAG	—	Not used
24	ECM	O	Spindle motor drive signal (Enforced mode output) 3-State	64	IPPLAG	—	Not used
25	ECS	O	Spindle motor drive signal (Servo error signal output)	65	FLAG	—	Not used
26	KICK	O	Kick pulse output	66	CLVS	—	Not used
27	TRD	O	Tracking drive output	67	CRC	—	Not used
28	FOD	O	Focus drive output	68	DEMPH		Not used
29	VREF	I	Reference voltage input pin for D/A output block (TVD,FOD,FBA,TBAL)	69	RESY	—	Not used
30	FBAL	O	Focus Balance adjust signal output	70	IOSEL	—	pull up
31	TBAL	O	Tracking Balance adjust signal output	71	TEST	—	pull up
32	FE	I	Focus error signal input(Analog input)	72	AVDD1	—	Power supply(Digital)
33	TE	I	Tracking error signal input(Analog input)	73	OUT L	O	Lch audio output
34	RF ENV	I	RF envelope signal input(Analog input)	74	AVSS1	—	Connected to GND
35	VDET	I	Vibration detect signal input(H:detect)	75	OUT R	O	Rch audio output
36	OFT	I	Off track signal input(H:off track)	76	RSEL	—	pull up
37	TRCRS	I	Track cross signal input	77	CSEL	—	Connected to GND
38	RFDET	I	RF detect signal input(L:detect)	78	PSEL	—	Connected to GND
39	BDO	I	BDO input pin(L:detect)	79	MSEL	—	Connected to GND
40	LDON	O	Laser ON signal output(H:on)	80	SSEL	—	Pull up

■ TA2057N (IC1) : FM/AM IF AMP & Detector

1.Block Diagrams

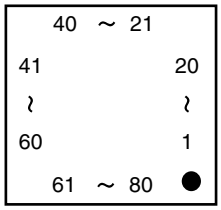


2.Pin Function

Pin No.	I/O	Symbol	Function	Pin No.	I/O	Symbol	Function
1	I	AM RF	AMRF signal input	13	O	Lch OUT	Output Lch
2		AM S.SENS		14	O	VCO	Voltage controlled terminal
3		FM S.SENS		15	O	LPF2	When voltage of terminal is MONO
4	-	AM OSC	AM local oscillation circuit				at "H" and ST at "L"
5	O	AM OSC OUT	AM local oscillation signal output	16	O	LPF1	When voltage of terminal is AM at
6	-	VCC	Power supply				"H" and FM at "L"
7	I	AGC	AGC voltage input terminal	17	I	MPX IN	Multi plex signal input
8	-	GND	Connect to GND	18	O	AM OUT	AM detection signal output
9	O	IF OUT	IF REQ signal output to IC2	19	O	FM OUT	FM detection signal output
10	O	TU IND	Indicator drive output when tuning	20	I	FM QUAD	Bypass to FMIF
11	O	ST IND	Stereo indicator output	21	I	AM IF IN	Input of AMIF signal
			"H"mono . "L"stereo	22	-	Vst	Fixed voltage output terminal
12	O	Rch OUT	Output Rch	23	O	AM MIX OUT	Output terminal for AM mixer
				24	I	FM IF IN	Input of FMIF signal

■ UPD780053GC-031(IC711):CD/VCD Control

1. Terminal layout



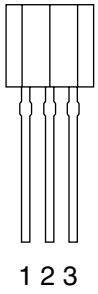
2Pin function

UPD780053GC-031

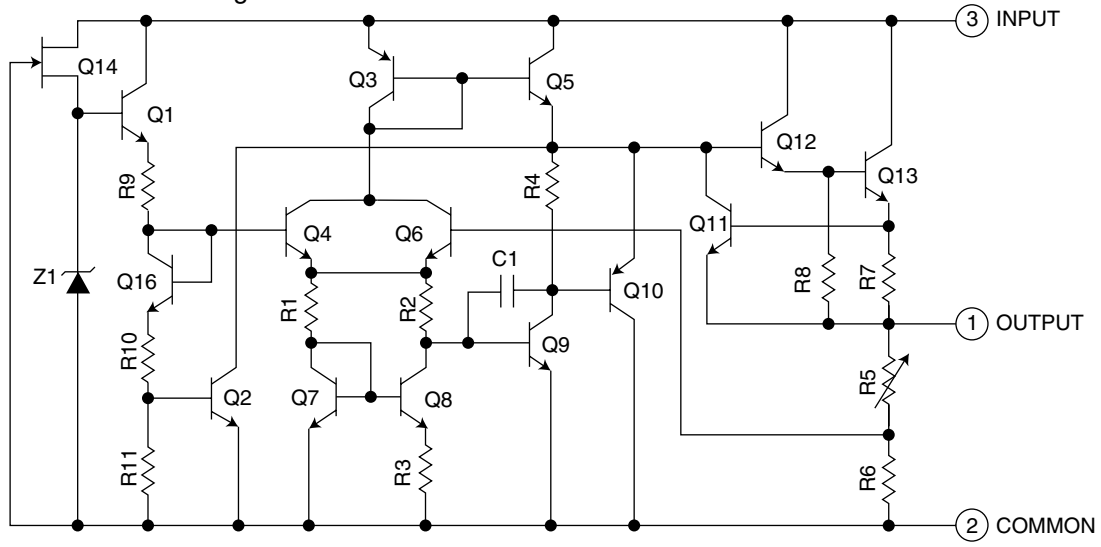
Pin No.	Symbol	I/O	Function
1	MLD	O	Micon command load signal output
2	MDATA	O	Micon command data output
3	MCLK	O	Micon command clock signal output(Data is latched at signal's rising point)
4	AVSS	-	GND
5	REST	I	Rest switch input
6	XRST	O	Reset signal input (L:Reset)
7	A-REF1	-	Connect to Vdd
8	SUBQ	I	Sub Q code input
9	NC	-	Non connection
10	SQCK	O	Outside clock for sub-code Q resister output
11	KCMD	-	GND
12	MSTAT	-	GND
13	KCLK	O	CD Micon control commend clock (Tuner:L)
14	OSOFF	I	OSD Input of deletion demand signal of display(L:OSD Off)
15	MRDY	I	CD Micon control Detection of state of command possible reception
16	NC	-	Non connection
17	SRDATA	O	Serial data output terminal
18	SRCLK	O	Serial clock output terminal
19～32	NC	-	Non connection
33	VSS1	-	GND
34～39	NC	-	Non connection
40	FCD	O	Function CD output terminal
41	MREQ	O	Transfer request data to IC111
42	VCDRST	O	VCD Reset signal output terminal
43	VCDEMP	O	VCD empty signal output terminal
44～59	NC	-	Non connection
60	CDMRST	O	CD Mechanism reset signal output terminal
61	STAT	I	CD Status signal input terminal
62	HREC		
63	HRDY		
64～66	NC	-	Non connection
67	V3S0	-	GND
68	VDD1	-	Connect to Vdd
69	X2	I	Input of X'tal oscillation circuit
70	X1	O	Output of 16.9344MHz X'tal oscillation circuit
71	IC	-	GND
72	XT2	-	Non connection
73	XT1	-	Connect to Vdd
74	VDD0	-	Connect to Vdd
75	AVREF0	-	GND
76～78	NC	-	Non connection
79	DMUTE	-	Connected to GND
80	DRMUTE	O	All BTL amplifiel outputs ON/OFF

■ KIA78S06P-T (IC702) : Regulator

1. Pin layout

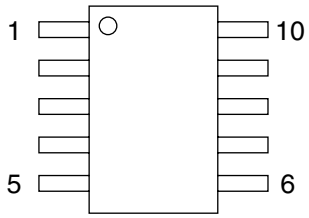


2. Block diagram



■ TA8409F-W (IC108) : Bridge driver

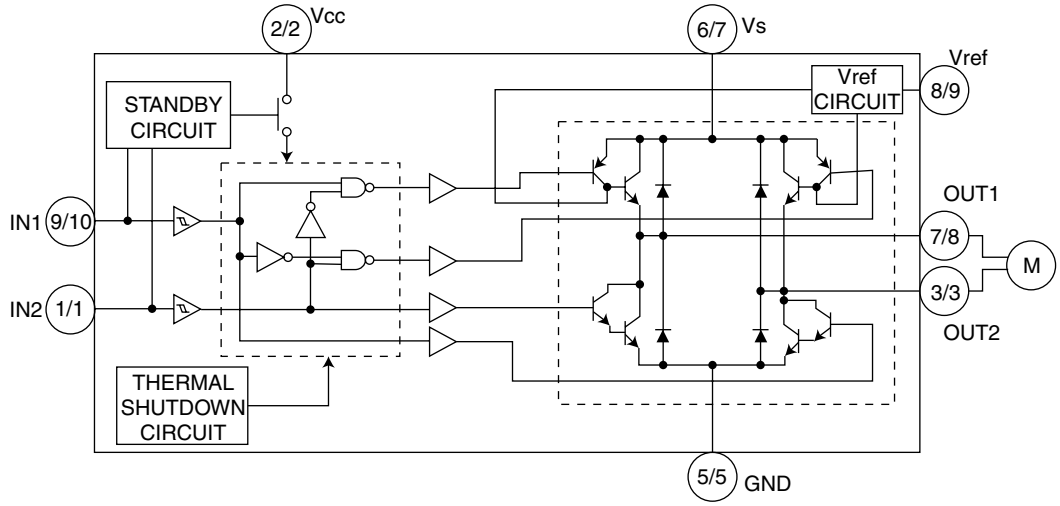
1. Pin layout



2. Pin function

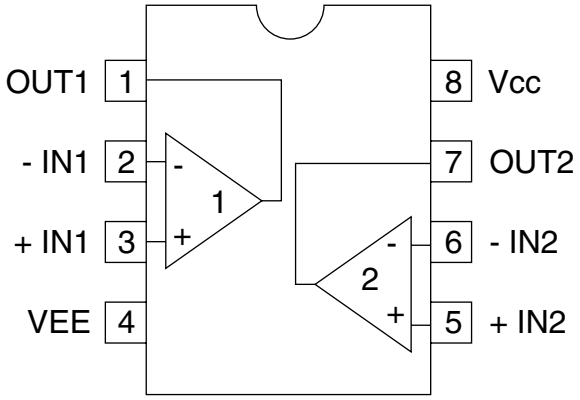
Pin No.	SYMBOL	FUNCTION
1	IN2	INput terminal
2	Vcc	Supply voltage terminal for logic
3	OUT2	Output terminal
4	NC	Non connection
5	GND	GND terminal
6	NC	Non connection
7	Vs	Supply voltage terminal for motor driver
8	OUT1	Output terminal
9	Vref	Reference voltage terminal for control circuit
10	IN1	Input terminal

3. Block diagram



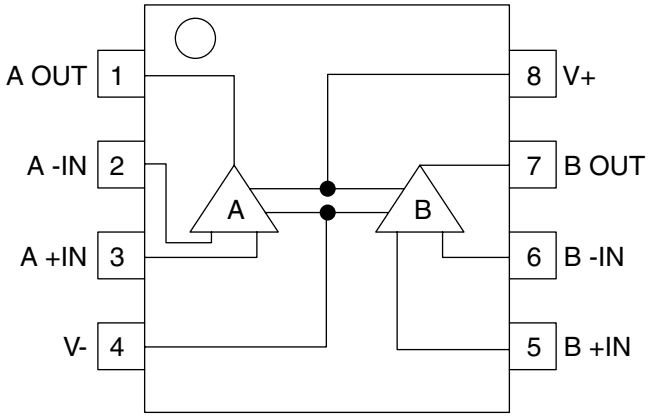
■ BA15218F-W (IC102) : Dual ope. amp.

1. Pin layout & Block diagram

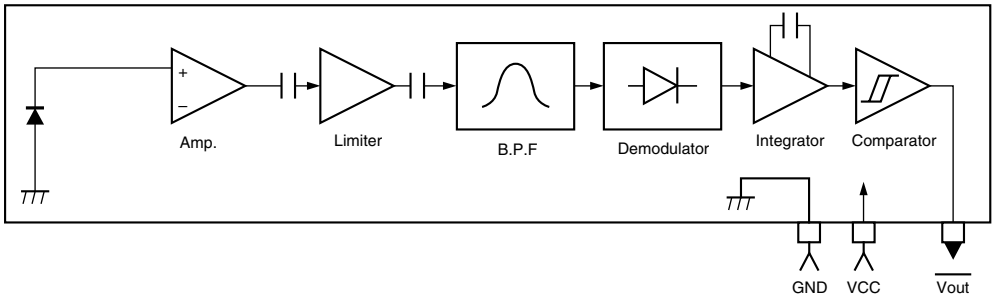


■NJM4580D-D (IC101) : Dual ope amp.

1. Pin layout & Block diagram

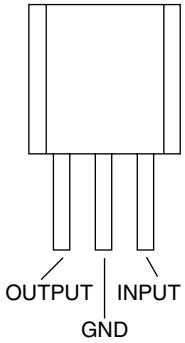


■GP1U271X (IC801) : Receiver for remote

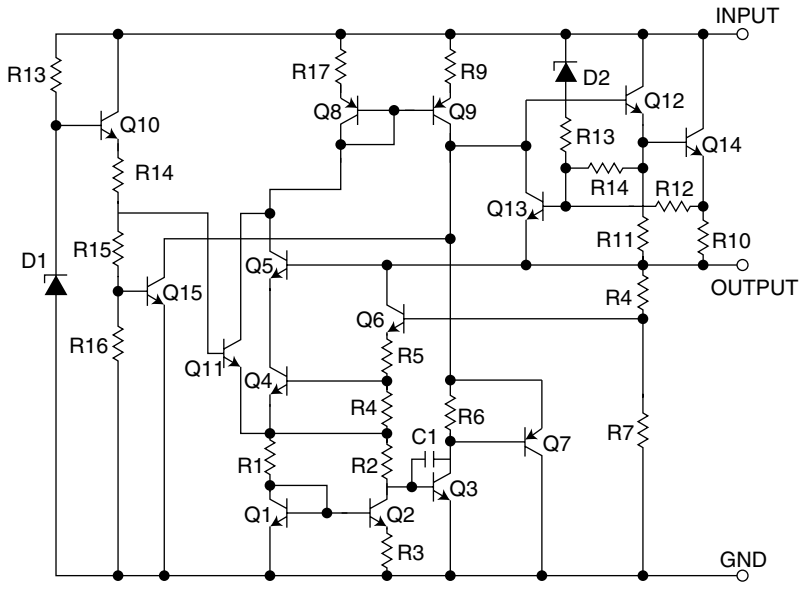


■ UPD78L5J-T (IC191) : Regulator

1. Pin layout

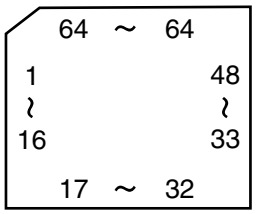


2. Block diagram



■ MN171601AK8J2(IC111):HOST Micro computer

1.Terminal layout

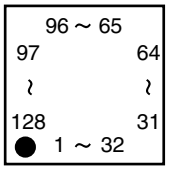


2.Pin function

Pin No.	Symbol	I/O	Function
1	480RST	O	Reset signal output.
2	MREQ	I	Input the transfer request data signal.
3	ACTINT	I	Interact 2 signal input.
4	GDET	I	CD-G detect terminal H:CD-G
5	GND	-	Connected to GND.
6	DTACK	I	Acknowledge signal input.
7	GND	-	Connect to GND.
8	GND	-	Connect to GND.
9	DIR	I/O	Input/Output control for IC114.
10	N/PAL	-	Not use.
11	ENCRST	O	Encoder riset signal output terminal.
12	W/R	I/O	Read/Write signal input/output.
13 ～ 15	HA0 ～ 2	O	Address signal output for MPEG LSI.
16	DS	O	Data strobe signal output.
17～24	HD0 ～7	I/O	Data terminal for MPEG LSI.
25～39	SA0～14	O	SRAM address signal output.
40	SCS	O	SRAM chip select signal output.
41～48	SD1～18	I/O	SRAM data Input /Output terminal .
49	SR/W	I/O	SRAM read/write signal input/output.
50	PAL60	-	Not use.
51	RESET	I	Reset signal input.
52	X1	-	Non connect.
53	X2	-	Non connect.
54	VSS	-	Connect to GND.
55	OSC2	-	Non connect.
56	OSC1	I	Clock input terminal.
57	VDD	-	Power supply.
58	HREQ	O	Communication signal output.
59	SRCLK	O	Clock signal for data request.
60	M2HDT	O	Serial data output.
61	M2MDT	I	Serial data input.
62	HRDY	O	Communication signal output.
63	VCD/G	O	Video swith swiching signal output.
64	PALCDG	O	CD-G PAL/NTSC clock select terminal.

■ CL480-F1(IC101):MPEG-1 AUDIO/VIDEO DECODER

1.Terminal layout

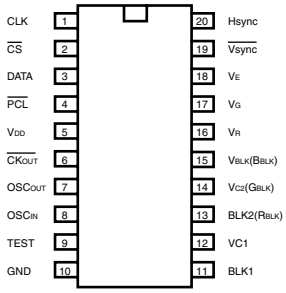


2.Pin function

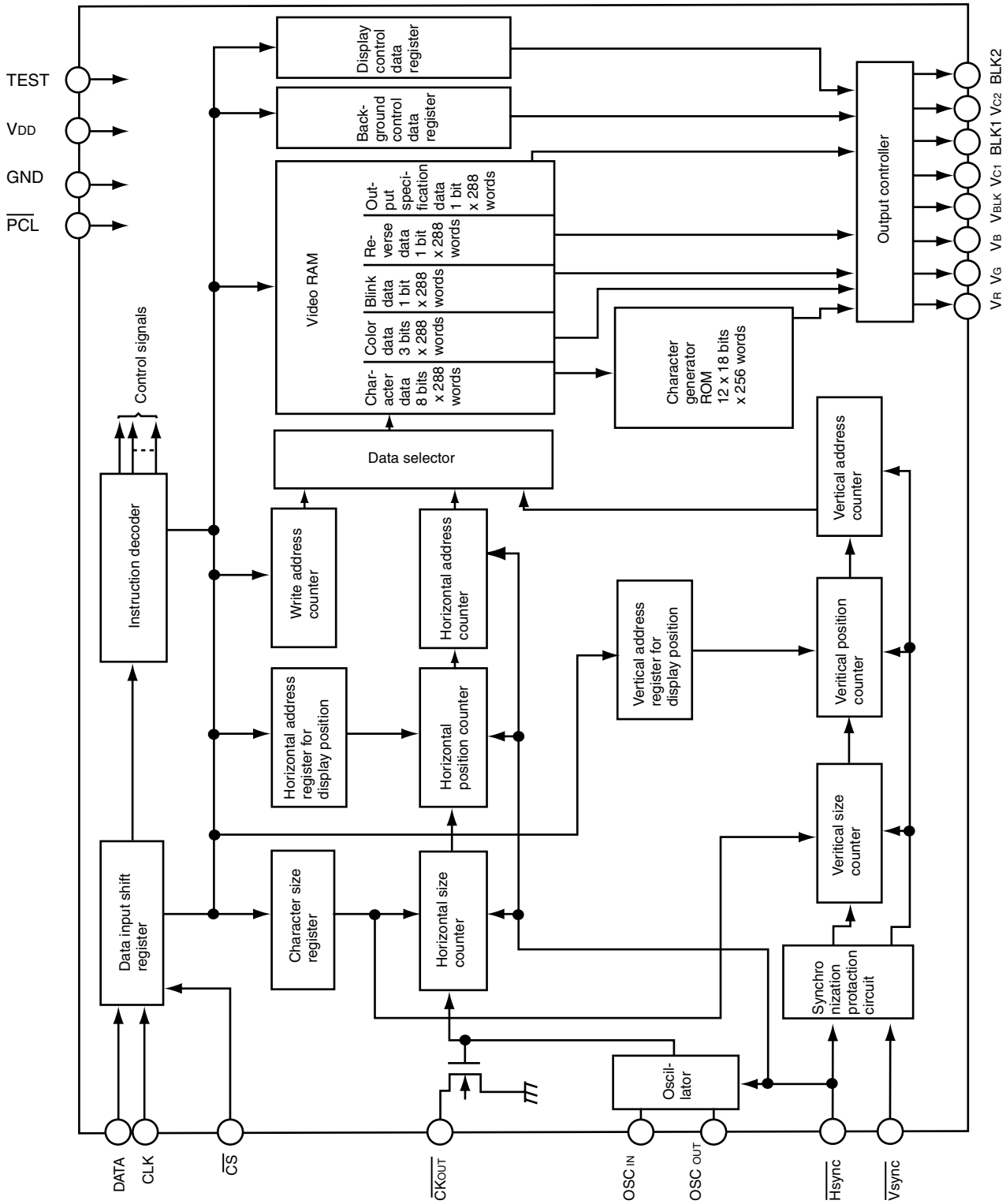
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	HA2	I	Host address.	78～80	VD10～12	O	Video data terminal(G24/Y24)
2	DS	I	Data strobe terminal.	81	IOVDD	-	Power supply for Input/Output.
3	W/R	I	I/O read terminal.	82～84	VD13～15	O	Video data terminal(G57/Y57)
4	IRQ	O	Interact terminal.	85	CKTVSS	-	Connect to GND.
5	DTACK	O	Acknowledge data output.	86～89	VD16～19	O	Video data terminal(B0B3)
6	HD0	I/O	Host data terminal.	90	IOVSS	-	Ground terminal for Input/Output.
7	IO VDD	-	Power supply for input/output.	91～94	VD20～23	O	Video data terminal(B47)
8,9	HD1,2	I/O	Host data terminal.	95	VSYNC	I/O	Vertical comparator/Composite
10	CKT VSS	-	Connected to GND.				comparator output.
11～15	HD3～7	I/O	Date data terminal.	96	HSYNC	I/O	Horizonatall synchronizing signal.
16	IOVSS	-	Ground terminal for Input/Output.	97	VOE	I	Video output enable signal.
17	TEST	I	Test terminal.	98	VCOVDD	-	Power supply of VCO.
18	XTLVSS	I	Oscillator ground terminal.	99	VCLK	I/O	Video clock terminal.
19	XTLIN	I	Oscillator input terminal.	100	VCOVSS	-	Ground of VCO.
20	XTLOUT	O	Oscillator output terminal.	101	RESET	I	Reset signal input.
21	XTLVDD	-	Power supply for oscillator.	102	IOVSS	-	Ground terminal for Input/Output.
22	CKTVDD	-	Power supply.	103	C2PO	I	Data error flag input.
23～28	MD0～5	I/O	DRAM data / ROM data terminal.	104	CDLRCK	I	L/R word clock input.
29	IOVDD	-	Power supply for Input/Output.	105	CDDATA	I	Bit serial data input.
30,31	MD6,7	I/O	DRAM data/ROM data terminal.	106	CDBCK	I	Bit clock output.
32,33	MCE01	O	Chip enable output for ROM bank.	107	DALRCK	O	L/R clock output.
34～37	MD8～11	I/O	DRAM data/ROM data terminal.	108	DADATA	O	Bit serial PCM audio signal output.
38	IOVSS	-	Ground terminal for Input/Output.	109	DABCK	O	Bit clock output.
39～42	MD12～15	I/O	DRAM data/ROM address terminal.	110	IOVDD	-	Power supply for Input/Output.
43	5VVDD	-	Power supply(+5V).	111	XCK	I	Bit clock input terminal.
44	LCAS	O	DRAM LCAS/ROM address terminal.	112	CKTVDD	-	Power supply.
45	LCASIN	I	DRAM LCAS input.	113	PIO12	O	Interact 2 signal output.
46	CKTVSS	-	Connect to GND.	114	PIO11	O	Non connect.
47	MWE	O	DRAM write enable signal output.	115	PIO10	I	Host enable signal input.
48	UCAS	O	DRAM UCAS/ROM address terminal.	116	PIO9	I	Boot ROM enable signal input.
49	IOVDD	-	Power supply for Input/Output.	117	PIO8	O	Non connect.
50	UCASIN		DRAM UCAS input terminal.	118	PIO7	O	DAC emphasis signal output.
51,52	RAS0,1	O	DRAM RAS0,1 terminal.	119	PIO6	I	CD-DA emphasis signal output.
53～57	MA9～5	O	DRAM data/ROM address terminal.	120	PIO5	O	Non connect.
58	IOVSS	-	Ground terminal for Input/Output.	121	PIO4	O	FMV detect signal output.
59～63	MA4～0	O	DRAM data/ROM address terminal.	122	PIO3	O	CD-DA video CD select signal
64	PIO0	O	ROM address extension terminal.				output Low:Video CD.
65	IOVDD	-	Power supply for Input/output.	123	5VVDD	-	Power supply (+5V).
66～72	VD0～6	O	Video data terminal	124	PIO2	O	Non connect.
			(R6/CrCb6/YCrCb066)	125	IOVSS	-	Ground for Input/Output.
73	IOVSS	-	Ground terminal for Input/Output.	126	PIO1	O	Non connect.
74～76	VD7～9	O	Video data terminal	127	HA0	-	Host address input.
			(R7/CrCb7/YCrCb7)(G0,1/Y0,1)	128	HA1	-	Host address input.
77	CKTVDD	-	Power supply.				

■ UPD6461GS-635(IC06):OSD

1.Terminal layout



2.Block diagram



3.Pin function

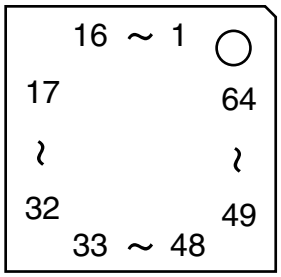
UPD6461GS-635

Pin No.	Symbol	Function	Description
1	CLK	Clock input	Input pin for the data read clock.The data input to the DATA pin is read at rising edges of the clock.
2	CS	Chip select input	Serial transfer is accepted when this pin is low.
3	DATA	Serial data input	Input pin for control cata. Data is read in synchronization with the clock input to the CLK pin.
4	PCL	Power-on clear	Pin used for the power-on clear function.After power-on.set this pin from low to high to initialize the IC.
5	VDD	Power supply	Power supply pin.
6	CKOUT	Clock output	N-ch open-drain output pin used to check the oscillation frequency
7 8	OSCout OSCin	LC oscillator input/output (OSCin:External clock input)	Input and output pins for the oscillator for generating a dot clock. Connect the oscillation coil and capacitors to these pins (When an external clock input is selected by specifying a mask option, input an external clock(synchronized with Hsync) to the OSC_{IN} pin, Leave OSC_{OUT} pin open.)
9	TEST	Test	Pin used for testing the IC.Usually, connect this pin to ground. The IC cannot enter test mode while this pin is connected to ground.
10	GND	Ground	Connect this pin to the system ground.
11	BLK1	Blanking signal output 1	Pin used to output the blanking signal for the video signal output from the V_{C1} pin. The blanking signal is high active. (When RGB separate blanking has been selected by specifying a mask option, This pin outputs the logical OR of R_{BLK}, G_{BLK},and B_{BLK}.)
12	VC1	Character signal output1	Pin used to output the blanking signal for the video signal output from the VC1 pin. The blanking signal is high active. (When RGB separate blanking has been selected by specifying a mask option,this pin outputs the logical OR of V_R, V_G and V_B.)
13	BLK2 (R_{BLK})	Blanking signal output2 (Blanking R)	Pin used to output the blanking signal for the video signal output from the V_{C2} pin. The blanking signal is high active. (This pin outputs the blanking signal for the video signal output from the V_R pin, The blanking signal is high active.)
14	VC2 (G_{BLK})	Character signal output2 (Blanking G)	Pin used to output a high-active character signal. (This pin outputs the blanking signal for the video signal output from the V_G pin. The blanking signal is high active.)
15	VBLK (B_{BLK})	Blanking signal output2 (Blanking B)	Pin used to output the blanking signal for the video signals output from the V_R,V_G,and V_B pins. The blanking signal is high active. (This pin outputs the blanking signal for the video signal output from the V_B pin, The blanking signal is high active.)
16 17 18	V_R V_G V_B	Character signal output	Pins used to output high-active character signals.
19	Vsync	Vertical synchronizing signal input	Input a low-active vertical synchronizing signal to this pin.
20	Hsync	Horizontal synchronizing signal input	Input a low-active horizontal synchronizing signal to this pin

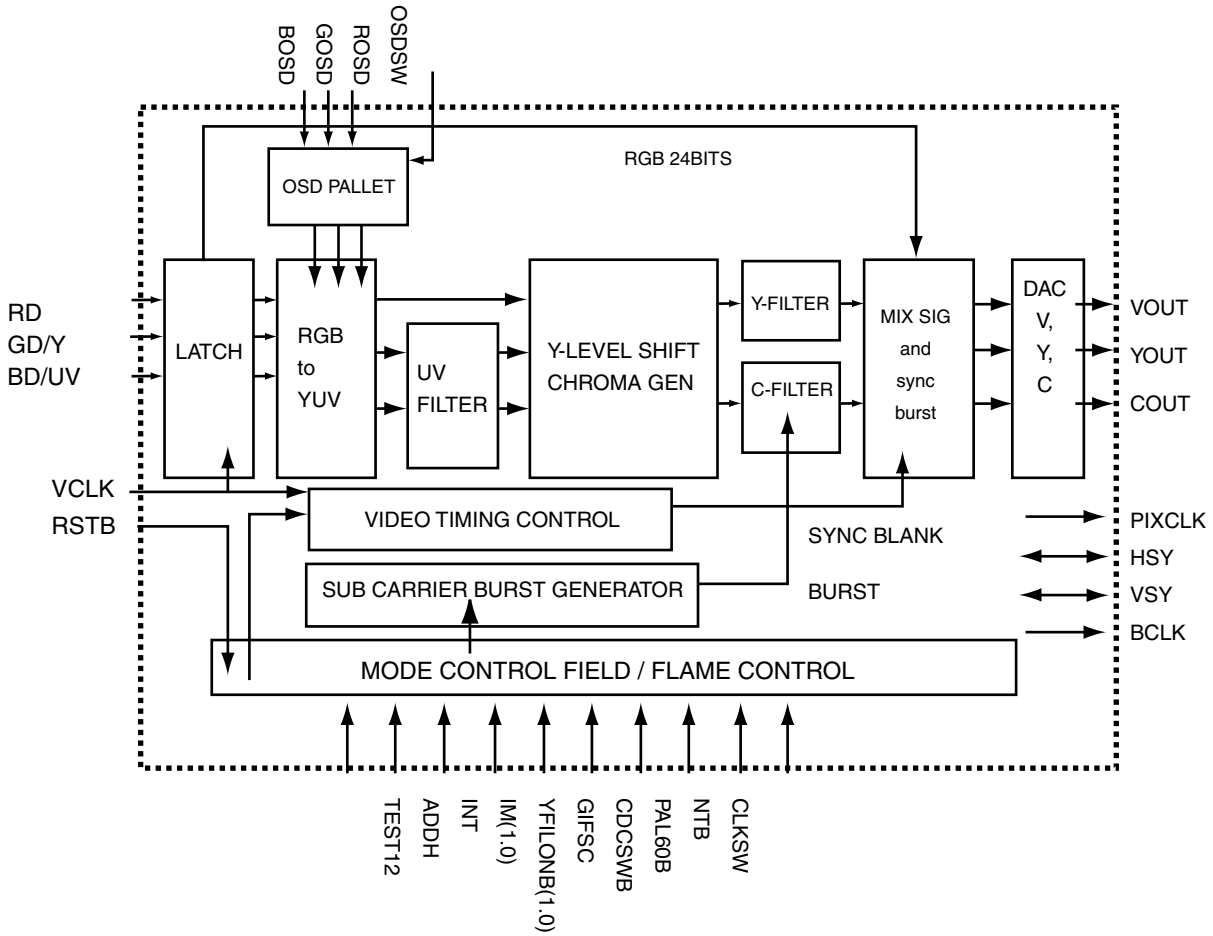
Symbols and functions indicated in parentheses for pins 13 to 15 apply when RGB separate blanking is selected with a mask option.

■ BU1424K(IC104):DIGITAL RGB ENCODER

1.Terminal layout



2.Block diagram



3.Pin function

BU1424K

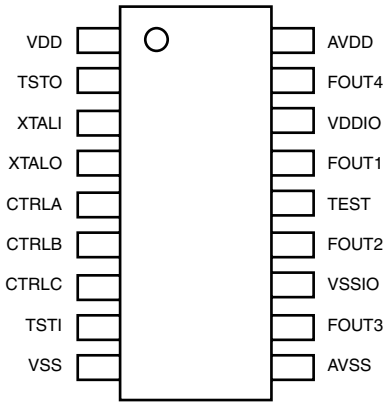
No.	NAME	FUNCTION		No.	NAME	FUNCTION	
1	BOSD	OSD BLUE DATA INPUT	*	33	SLABEB	SELECT MASTER/SLAVE	*
2	GD0/Y0	GREEN DATA Bit0(LSB)		34	ADDH	+0.5/-0.5LINE at NON-INTER	*
3	GD1/Y1	GREEN DATA Bit1		35	VREF-C	DAC BIAS	
4	GD2/Y2	GREEN DATA Bit2		36	CGND	CHROMA OUTPUTGROUND	
5	GD3/Y3	GREEN DATA Bit3		37	COUT	CHROMA OUTPUT	
6	GD4/Y4	GREEN DATA Bit4		38	VGND	Composite Output Ground	
7	GD5/Y5	GREEN DATA Bit5		39	VOUT	COMPOSITE OUTPUT	
8	GD6/Y6	GREEN DATA Bit6		40	AVSS	Analog Ground (DAC,VREF)	
9	GND	DIGITAL GROUND		41	AVDD	ANALOG(DAC) VDD	
10	GD7/Y7	GREEN DATA Bit7(MSB)		42	IR	REFERENCE RESISTOR	
11	BD0/UV0	BLUE DATA Bit0(LSB)		43	AVDD	ANALOG(VREF) VDD	
12	BD1/UV1	BLUE DATA Bit1		44	YGND	Luminance Output Ground	
13	BD2/UV2	BLUE DATA Bit2		45	YOUT	Luminance Output	
14	BD3/UV3	BLUE DATA Bit3		46	G4FSC	4FSC/32FSC at PALCD-G	*
15	OSDSW	OSD ENABLE/DISABLE	*	47	YFILON2B	Y-FILSEL THROU/FILON2	**
16	CDGSWB	SELECT Video-CD/CD-G		48	YCOFF	DAC(YOUT,COUT)OFF	*
17	BD4/UV4	BLUE DATA Bit4		49	YFILON1B	Y-FILSEL THROU/FILON1	**
18	BD5/UV5	BLUE DATA Bit5		50	PAL60B	NORMAL/PAL60 at PALMODE	**
19	BD6/UV6	BLUE DATA Bit6		51	VCLK	Video Clock Input	
20	BD7/UV7	BLUE DATA Bit7(MSB)		52	RSTB	NORMAL/RESET	**
21	GND	DIGITAL GROUND		53	CLKSW	SEL*1CLK/*2CLK	
22	NTB	SELECT NISC/PAL MODE		54	RD0	RED DATA Bit(LSB)	*
23	IM0	SELECT YUV/RGB	*	55	RD1	RED DATA Bit1	*
24	IM1	SELECT DAC/NORMAL	*	56	RD2	RED DATA Bit2	*
25	TEST1	normally pull down to GND	*	57	ROSD	OSD RED DATA INPUT	*
26	TEST2	SELECT U/V TIMING	*	58	RD3	RED DATA Bit3	*
27	VSY	V-SYNC INPUT or OUTPUT		59	RD4	RED DATA Bit4	*
28	HSY	H-SYNC INPUT or OUTPUT		60	RD5	RED DATA Bit5	*
29	PIXCLK	1/2freq of BCLK		61	VDD	DIGITAL VDD	
30	BCLK	INTERNAL CLOCK OUTPUT		62	RD6	RED DATA Bit6	*
31	VDD	DIGITAL VDD		63	RD7	RED DATA Bit7	*
32	INT	Interface /Non-interface		64	GOSD	OSDGREEN DATA INPUT	*

* The pin built-in pull-down resistor

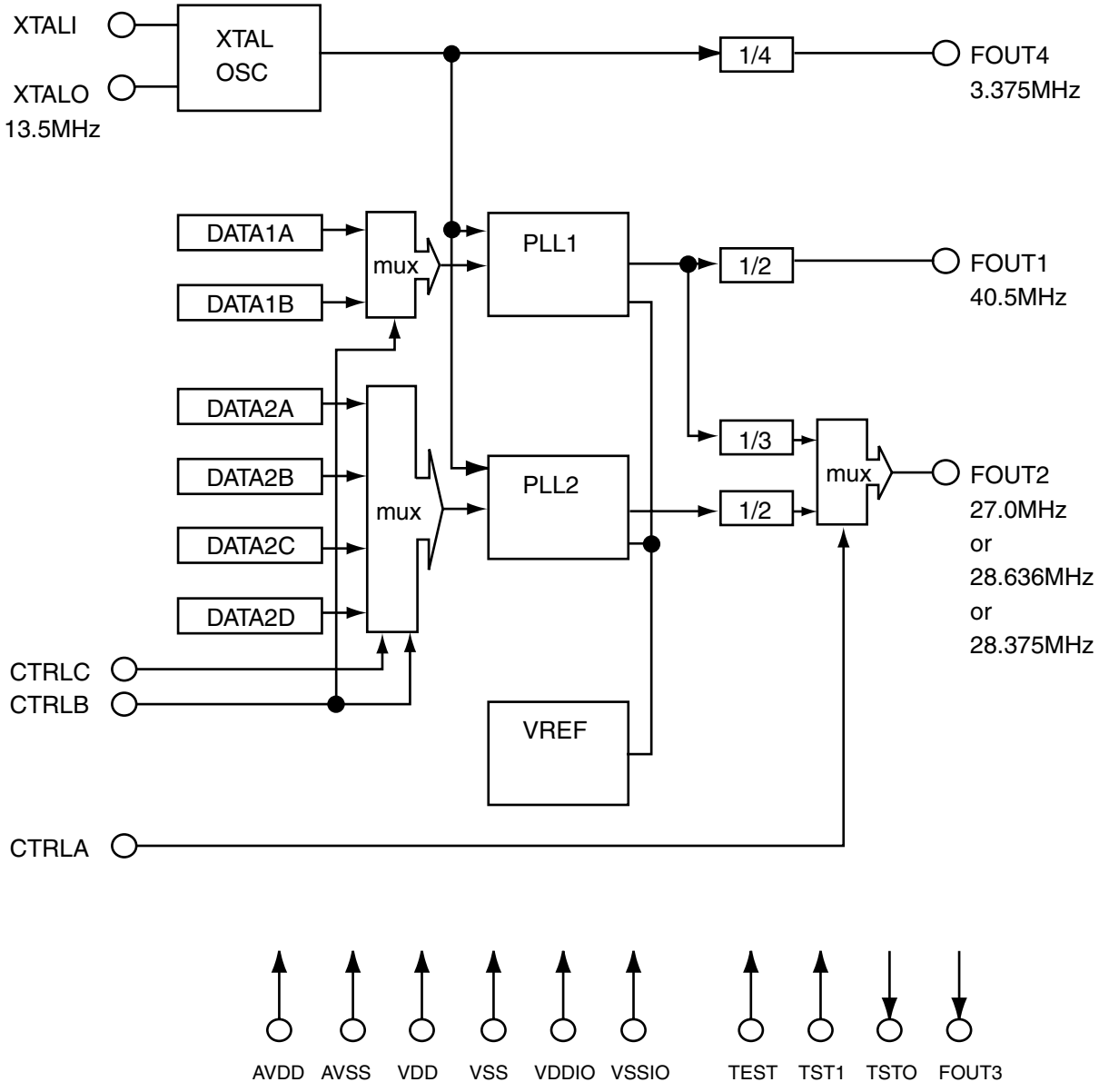
** The pin built-in pull-up resistor

■ BU2173F(IC105):VCO

1.Terminal layout



2.Block diagram



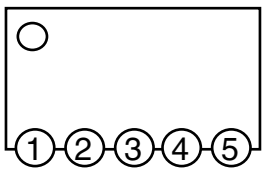
3.Function

BU2173F(IC105)

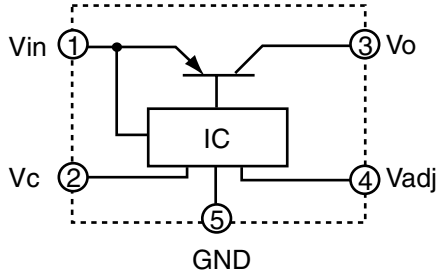
Pin No.	Symbol	Function
1	VDD	Digital VDD
2	TSTO	Use open this Pin for NORMAL OPERATION
3	XTALI	Reference oscillation input
4	XTALO	Reference oscillation output
5	CTRLA	Frequency select for V-CD / CD-G
6	CTRLB	Force H for NORMAL OPERATION
7	CTRLC	RAL / NTSC select for CD-G MODE
8	TSTI	Force L for NORMAL OPERATION
9	VSS	Digital GND
10	AVSS	Analog GND
11	FOUT3	Use open this Pin for NORMAL OPERATION
12	VSSIO	I / O GND
13	FOUT2	CLOCK OUTPUT (2)
14	TEST	Force L for NORMAL OPERATION
15	FOUT1	CLOCK OUTPUT (1)
16	VDDIO	I / O VDD
17	FOUT4	CLOCK OUTPUT (4)
18	AVDD	Analog VDD

■ PQ20VZ11(IC107):Reguratpr

1.Terminal layout

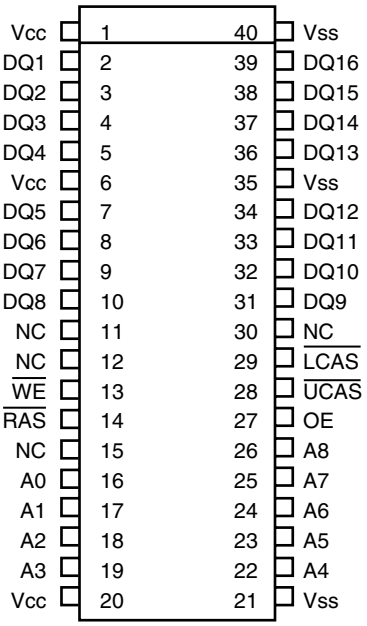


2.Block daigram



■ V53C16258HK40(IC103):4M DRAM

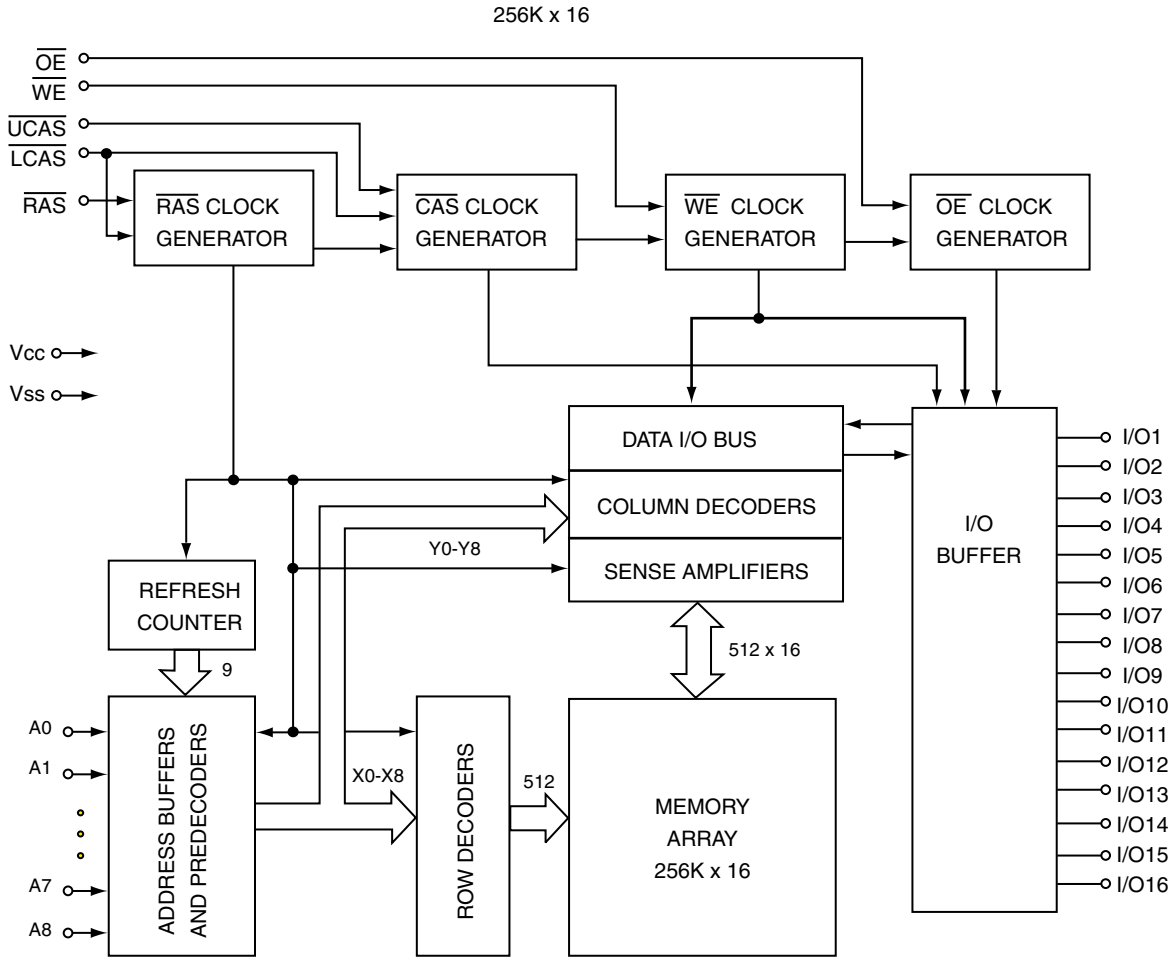
1.Terminal layout



2.Pin function

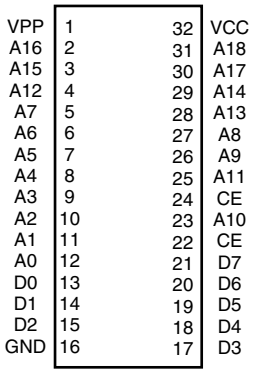
Symbol	Function
A0-A8	Adress Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe / Upper Byte Control
$\overline{LCAS}$	Column Address Streobe / Lower Byte Control
$\overline{WE}$	Write Enable
OE	Output Enable
DQ1-DQ16	Data Input, Output
Vcc	+5V Supply
Vss	0V Supply
NC	No Connect

3.Block diagram

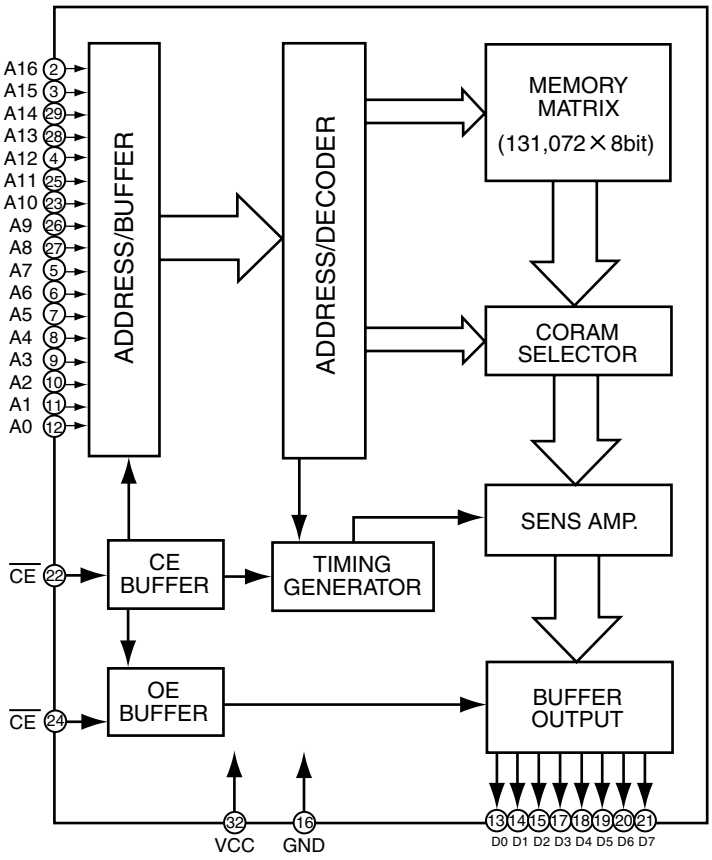


■ LH531HEG(IC102)

1.Terminal Layout



2.Block diagram

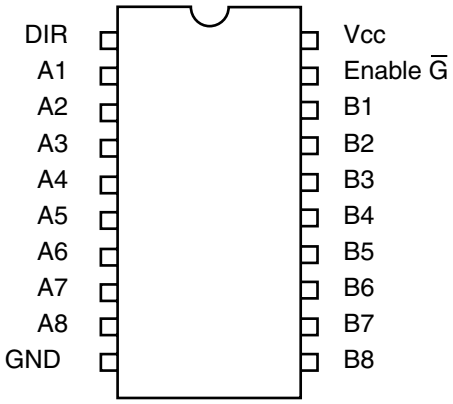


3.Pin Function

Pin No.	Symbol	I/O	Function
1	VPP	-	Power supply.
2	A16	I	Adress input.
3	A15	I	Adress input.
4	A12	I	Adress input.
5 ～12	A7A0	I	Adress input.
13～15	D0D2	O	Data output.
16	GND	-	Connect to GND
17～21	D3D7	O	Data output.
22	CE	I	Chip enable input.
23	A10	I	Adress input.
24	CE	I	Chip enable input.
25	A11	I	Adress input.
26,27	A9,A8	I	Adress input.
28,29	A13,A14	I	Adress input.
30,31	D17,D18	O	Data output.
32	VCC	-	Power supply.

■ HD74HCT245FP(IC114):EEP ROM

1.Terminal layout



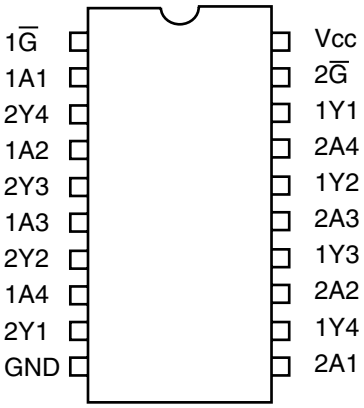
2.Pin function

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H : High level
L : Low level
X : Irrelevant

■ HD74HCT244FP(IC113):EEP ROM

1.Terminal layout



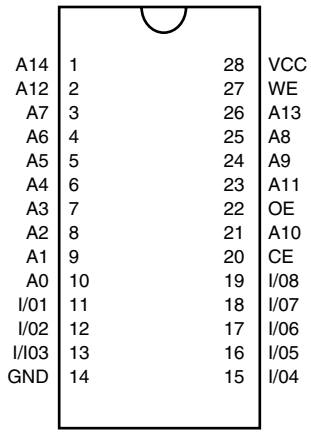
2.Pin function

INPUTS		OUTPUT
1$\overline{G}$,2$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

H : High Level
L : Low Level
X : Irrelevant
Z : High Impedance

■ TC55257DFL85L(IC112):256 Bit Static RAM

1.Terminal layout



2.Pin function

Pin No.	Symbol	I/O	Function
1 ～10	A14,12,17～ 0	I	Address input terminal
11～13	I/O1 ～ I/O3	I/O	Data input / output terminal
14	GND	-	Connected to GND
15～19	I/O4 ～ I/O8	I/O	Data input / output terminal
20	CE	I	Chip enable terminal
21	A10	I	Address input terminal
22	OE	I	Output enable terminal
23～26	A11,9,8,13	I	Address input terminal
7	WE	I	Write enabale terminal
28	VCC	-	Power supply

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